High-speed, 10-Bit, 125MSPS, CMOS Digital-to-Analog Converter

FEATURES

- 125 MSPS Update Rate
- 10-Bit Resolution
- Differential Current Outputs: 2 mA to 20 mA
- SFDR at 100MHz clock with 1MHz output: 64 dBc
- Fast Settling: 35 ns Full-Scale Settling to 0.1%
- On-Chip 1.10 V Reference
- Edge-Triggered Latches
- Power Dissipation: 115 mW @ 5 V
- Single +5 V or +3 V Supply Operation
- Green, 28-Lead TSSOP Package

APPLICATIONS

- Communications Transmit Channel
- Signal Reconstruction
- Direct Digital Synthesis (DDS)
- Instrumentation
- Video Reconstruction

PRODUCT HIGHLIGHTS

- Manufactured on a CMOS process, the 3PD5651E uses a proprietary switching technique that enhances dynamic performance well beyond 8- and 10-bit video DACs.
- On-chip, edge-triggered input CMOS latches readily interface to +3V and +5V CMOS logic families. The 3PD5651E can support update rates up to 125MSPS.
- A flexible single-supply operating range of +2.7V to +5.5V and a wide full-scale current adjustment span of 2mA to 20mA allows the 3PD5651E to operate at reduced power levels (i.e., 45mW) without any degradation in dynamic performance.
- A temperature compensated, 1.10V bandgap reference is included on-chip providing a complete DAC solution. An external reference may be used.
- The current output(s) of the 3PD5651E can easily be configured for various single-ended or differential applications.

PRODUCT DESCRIPTION

The 3PD5651E offers exceptional AC and DC performance while supporting update rates up to 125 MSPS. The 3PD5651E's flexible single-supply operating range of +2.7V to +5.5V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to 45mW, without a significant degradation in performance, by lowering the full-scale current output. In addition, a power-down mode reduces the standby power dissipation to approximately 20mW.

The 3PD5651E is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3V and +5V CMOS logic families.

The 3PD5651E is a current-output DAC with a nominal full-scale output current of 20mA and > 100kΩ output impedance.

Differential current outputs are provided to support single-ended or differential applications. The current outputs may be directly tied to an output resistor to provide two complementary, single-ended voltage outputs. The output voltage compliance range is 1.25V.

The 3PD5651E contains a 1.10V on-chip reference and reference control amplifier, which allows the full-scale output current to be simply set by a single resistor. The 3PD5651E can be driven by a variety of external reference voltages.

The 3PD5651E's full-scale current can be adjusted over a 2mA to 20mA range without any degradation in dynamic performance. Thus, the 3PD5651E may operate at reduced power levels or be adjusted over a 20dB range to provide additional gain ranging capabilities.

The 3PD5651E is available in 28-Lead TSSOP package. It is specified for operation over the industrial temperature range.

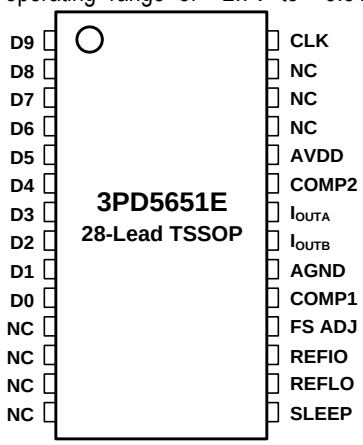


Figure 1. Pin Configuration

FUNCTIONAL BLOCK DIAGRAM

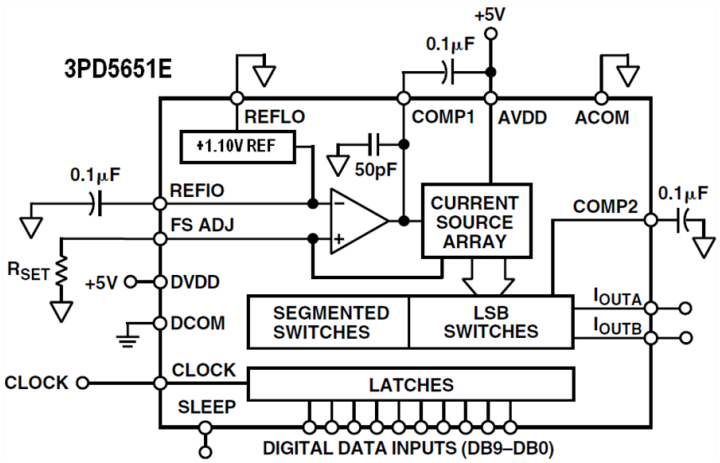


Figure 2. Functional Block Diagram

PIN CONFIGURATION

Pin No.	Name	Description
1	DB9	Most Significant Data Bit (MSB).
2–9	DB8–DB1	Data Bits 1–8.
10	DB0	Least Significant Data Bit (LSB).
11–14,25	NC	No Internal Connection
15	SLEEP	Power-Down Control Input. Active High. Contains active pull-down circuit, thus may be left unterminated if not used.
16	REFLO	Reference Ground when Internal 1.10 V Reference Used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., Tie REFLO to AVDD). Serves as 1.10 V reference output when internal reference activated (i.e., Tie REFLO to ACOM). Requires 0.1 μF capacitor to ACOM when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust.
19	COMP1	Bandwidth/Noise Reduction Node.Add 0.1 μF to AVDD for optimum performance.
20	ACOM	Analog Common.
21	I_{OUTB}	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	I_{OUTA}	DAC current Output. Full-scale current when all data bits are 1s.
23	COMP2	Internal Bias Node for Switch Driver Circuitry. Must decouple to ACOM with 0.1 μF capacitor or larger.
24	AVDD	Analog Supply Voltage (+2.7 V to +5.5 V).
25	NC	
26	NC	
27	NC	
28	CLK	Clock Input. Data latched on positive edge of clock of 3PD5651E.

ORDERING GUIDE

Model	Temperature Range	Package	MSL	Transport Media, Quantity
3PD5651E	–40°C to +85°C	28-Lead TSSOP	3	Tape and Reel, 2500

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±1000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±500	V

ABSOLUTE MAXIMUM RATINGS *

Parameter	With Respect to	Min	Typ.	Max	Units
VDD	ACOM	–0.3		6.5	V
CLOCK, SLEEP	ACOM	–0.3		AVDD+ 0.3	V
Digital Inputs	ACOM	–0.3		AVDD+0.3	V
I_{OUTA}, I_{OUTB}	ACOM	–0.3		1.8	V
COMP1,	ACOM	–0.3		AVDD+ 0.3	V
COMP2	ACOM	–0.3		1.8	V
FS ADJ	ACOM	–0.3		1.8	
REFIO,	ACOM	–0.3		AVDD+ 0.3	V
REFLO	ACOM	–0.3		0.3	V
Junction Temperature				125	°C
Storage Temperature		–65		150	°C
Lead Temperature (10 sec)				300	°C
Θ_{JA}	Thermal Resistance		97.9		°C/W
Θ_{JC}	of 28-Lead TSSOP		14.0		°C/W

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS

DC SPECIFICATIONS
(T_{MIN} to T_{MAX}, AVDD = +5V, I_{OUTFS} = 20mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
MONOTONICITY	GUARANTEED OVER SPECIFIED TEMPERATURE RANGE			
DC ACCURACY[1]				
Integral Linearity Error (INL)	-2.3	± 1/2	-2.3	LSB
Differential Nonlinearity (DNL)	-2	± 1/4	2	LSB
ANALOG OUTPUT				
Offset Error	-0.6		0.6	% of FSR
Gain Error(Without Internal Reference)		± 2		% of FSR
Gain Error (With Internal Reference)	–15	± 2	+15	% of FSR
Full-Scale Output Current[2]	2		20	mA
Output Compliance Range (single end)	0.2		0.8	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	0.89	1.075	1.26	V
REFERENCE INPUT				
Input Compliance Range			1.25	V
Reference Input Resistance		1		M
TEMPERATURE COEFFICIENTS				
Offset Drift		10		ppm of FSR/°C
Gain Drift (With Internal Reference)		± 50		ppm of FSR/°C
POWER SUPPLY				
Supply Voltages of AVDD[5]	2.7	5	5.5	V
Analog Supply Current (I_{AVDD})		21	30	mA
Power Dissipation (5 V, I_{OUTFS} = 20 mA)		110		mW
OPERATING RANGE	–40		+85	°C

NOTES
1. Measured at I_{OUTA}, driving a virtual ground.
2. Nominal full-scale current, I_{OUTFS}, is 32 x the I_{REF} current. Design valid.
3. Use an external buffer amplifier to drive any external load.
4. Reference bandwidth is a function of external cap at COMP1 pin.
5. For operation below 3 V, it is recommended that the output current be reduced to 12mA or less to maintain optimum performance.

DYNAMIC SPECIFICATIONS (Specifications subject to change without notice.)
(T_{MIN} to T_{MAX}, AVDD = +5V, I_{OUTFS} = 20mA, Differential Output, 30Ω Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})		125		MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY TO NYQUIST				
Total Harmonic Distortion				
f_{CLOCK} = 100 MSPS, f_{OUT} = 1 MHz		-62		dBc
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 100 MSPS, f_{OUT} = 1 MHz		64		dBc
Signal Noise Ratio				
f_{CLOCK} = 100 MSPS, f_{OUT} = 1 MHz		52		dBc

NOTES (Specifications subject to change without notice.)
1. Measured single ended into 50Ω load.

DIGITAL SPECIFICATIONS (Specifications subject to change without notice.)
(T_{MIN} to T_{MAX}, AVDD = +5V, I_{OUTFS} = 20mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ AVDD = +5 V	4	5		V
Logic "1" Voltage @ AVDD = +3 V	2.4	3		V
Logic "0" Voltage @ AVDD = +5 V		0	0.6	V
Logic "0" Voltage @ AVDD = +3 V		0	0.6	V
Logic "1" Current		1		uA
Logic "0" Current		1		uA
Input Capacitance		5		pF
Input Setup Time (t_S)		2		ns
Input Hold Time (t_H)		1.5		ns
Latch Pulsewidth (t_{LPW})		3.5		ns

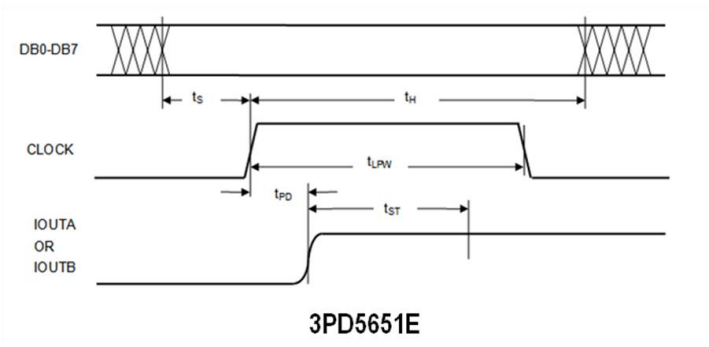


Figure 3. Timing Diagram

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0mA output is expected when the inputs are all 0s. For I_{OUTB}, 0mA output is expected when all inputs are set to 1s.

Gain Error (the difference between the actual and ideal output span)
The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum changes in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the RMS amplitude of the output signal and the peak spurious signal over the specified bandwidth

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio
SINAD is the ratio of the RMS value of the measured output signal to the RMS sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

Total Harmonic Distortion
THD is the ratio of the RMS sum of the first six harmonic components to the RMS value of the measured output signal. It is expressed as a percentage or in decibels.

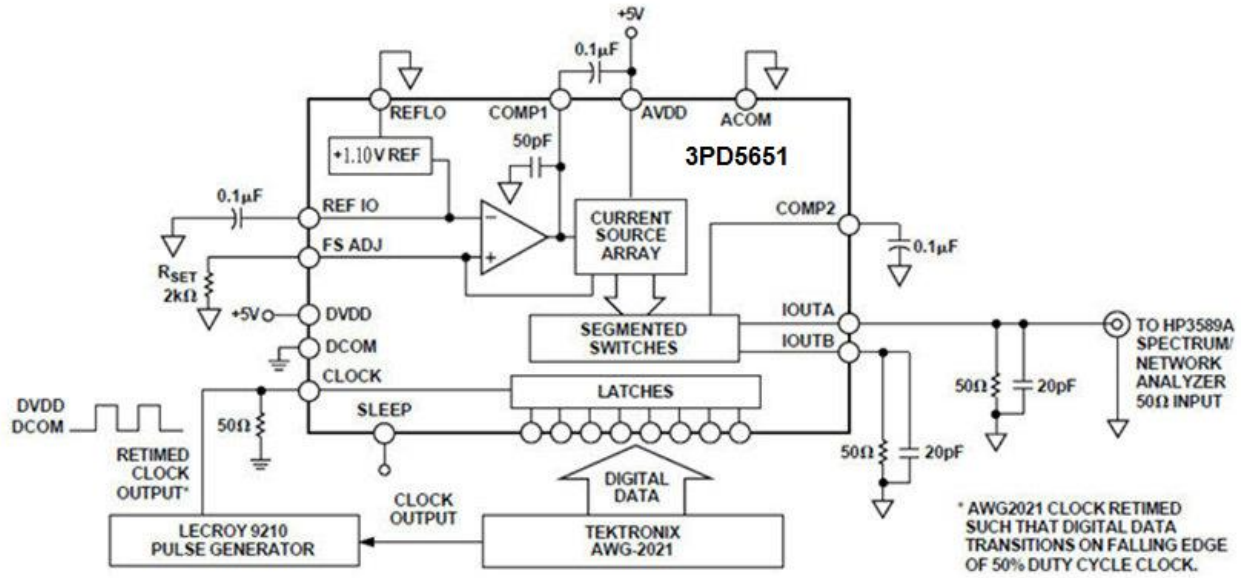


Figure 4. Basic AC Characterization Test Setup

TYPICAL CHARACTERIZATION CURVES

AVDD = +3 V, 50Ω Doubly Terminated Load, Single-Ended Output, I_{OUTA}, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.

FUNCTIONAL DESCRIPTION

The 3PD5651E consists of a large PMOS current source array capable of providing up to 20mA of total current. The array is divided into 32 equal currents that make up the five most significant bits (MSBs). The remaining 3 LSBs are also implemented with equally weighted current sources whose sum total equals 7/8th of an MSB current source. Implementing the upper and lower bits with current sources helps maintain the DAC's high output impedance (i.e. > 100 kW). All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance.
The analog and digital sections of the 3PD5651E have separate power supply inputs (i.e., AVDD) that can operate independently over a 2.7 volt to 5.5 volt range. The digital section, which is capable of operating up to a 125MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.10V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2mA to 20mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

DAC TRANSFER FUNCTION

The 3PD5651E provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 255), while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} are a function of both the input code and I_{OUTFS} and can be expressed as:

$I_{OUTA} = (DAC\ CODE/256) * I_{OUTFS}$

$I_{OUTB} = (255 - DAC\ CODE)/256 * I_{OUTFS}$

where *DAC CODE* = 0 to 255 (i.e., Decimal Representation).

As previously mentioned, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 * I_{REF}$$

Where $I_{REF} = V_{REFIO}/R_{SET}$

$V_{OUTA} = I_{OUTA} * R_{LOAD}$

$V_{OUTB} = I_{OUTB} * R_{LOAD}$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, V_{DIFF}, appearing across I_{OUTA} and I_{OUTB} is:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) * R_{LOAD}$$

Substituting the values of I_{OUTA}, I_{OUTB}, and I_{REF}; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2\ DAC\ CODE - 255)/256\}/ * (32\ R_{LOAD}/R_{SET}) * V_{REFIO}$$

VOLTAGE REFERENCE AND CONTROL AMPLIFIER

The 3PD5651E contains an internal 1.10V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is selected. If REFLO is tied to ACOM, as shown in Figure 14, the internal reference is activated and REFIO provides a 1.10 V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1μF or greater from REFIO to REFLO. Note that REFIO is not designed to drive any external load. It should be buffered with an external amplifier having an input bias current less than 100nA if any additional loading is required.

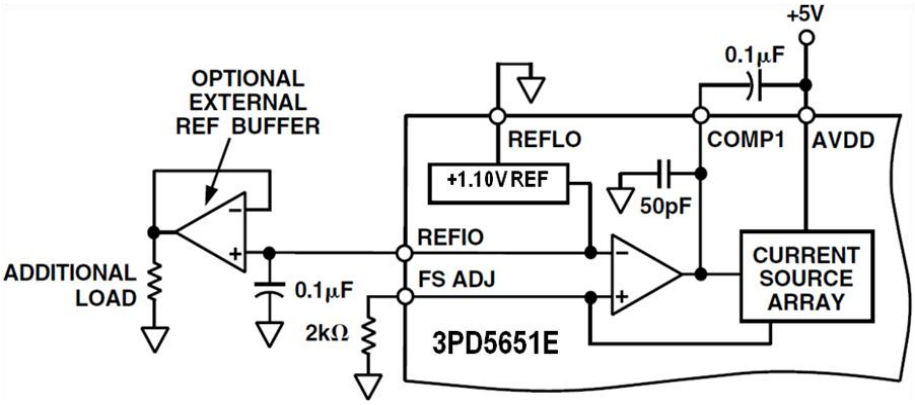


Figure 14. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may then be applied to REFIO as shown in Figure 15. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1μF compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

The small signal bandwidth of the reference control amplifier is approximately 1.8MHz and can be reduced by connecting an external capacitor between COMP1 and AVDD. The output of the control amplifier, COMP1, is internally compensated via a 50pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance further limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier. If I_{REF} is fixed for an application, a 0.1μF ceramic chip capacitor is recommended.

I_{REF} can be varied for a fixed R_{SET} by disabling the internal reference and varying the common-mode voltage over its compliance range of 1.25V to 0.10V. REFIO can be driven by a single-supply amplifier or DAC, thus allowing I_{REF} to be varied for a fixed R_{SET}. Since the input impedance of REFIO is approximately 1MΩ, a simple R-2-R ladder DAC configured in the voltage mode topology may be used to control the gain. Note another 3PD5651E could also be used as the gain control DAC since it can also provide a programmable unipolar output up to 1.2V.

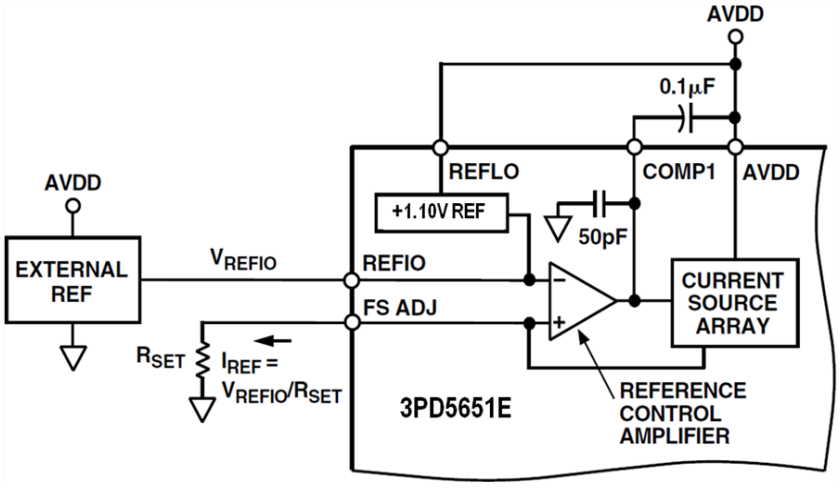


Figure 15. External Reference Configuration

ANALOG OUTPUTS AND OUTPUT CONFIGURATIONS

The 3PD5651E produces two complementary current outputs, I_{OUTA} and I_{OUTB}, which may be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC TRANSFER FUNCTION section. Figure 16 shows the 3PD5651E configured to provide a positive unipolar output range of approximately 0V to +0.5V for a double terminated 50Ω cable for a nominal full-scale current, I_{OUTFS}, of 20mA. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB} and is equal to 25Ω. The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to.

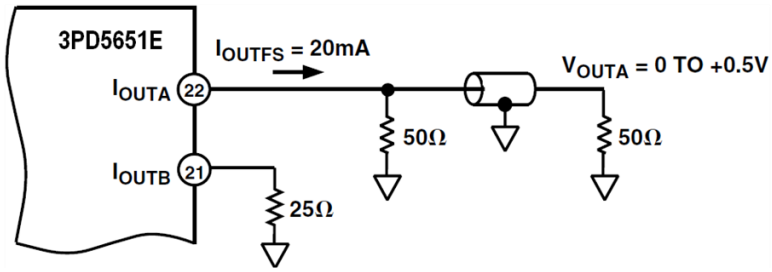


Figure 16. 0 V to +0.5 V Unbuffered Voltage Output

Alternatively, an amplifier could be configured as an I-V converter thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. Figure 17 shows a buffered singled-ended output configuration in which the op amp, U1, performs an I-V conversion on the 3PD5651E output current. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS}, since the signal current U1 will be required to sink and will be subsequently reduced. Note, the ac distortion performance of this circuit at higher DAC update rates may be limited by U1's slewing capabilities.

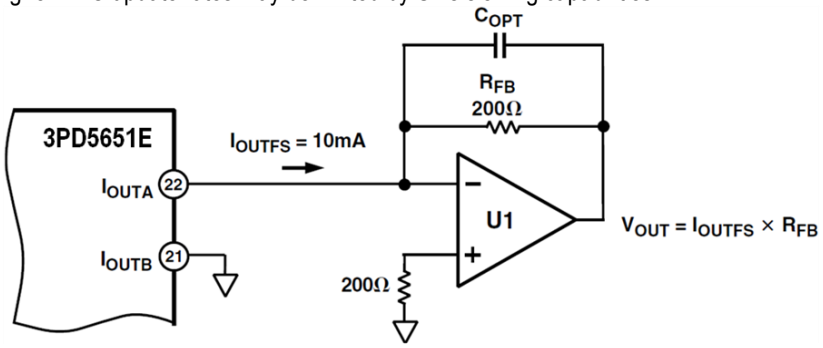


Figure 17. Unipolar Buffered Voltage Output

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25V for an I_{OUTFS} = 20mA to 1.00V for an I_{OUTFS} = 2mA. Applications requiring the 3PD5651E's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend up to its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the 3PD5651E's linearity. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} may also be converted to a single-ended voltage via a transformer or differential amplifier configuration. Refer to the DIFFERENTIAL OUTPUT CONFIGURATION section for more information.

DIGITAL INPUTS

The 3PD5651E's digital input consists of eight data input pins and a clock input pin. The 10-bit parallel data inputs follow standard positive binary coding where DB9 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). The digital interface is implemented using an edge-triggered master slave latch. The 3PD5651 output is updated following the rising edge as shown in Figure 3 and is designed to support a clock rate as high as 125MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse-width. The setup-and-hold times can also be varied within the clock cycle as long as the specified minimum times are met; although the location of these transition edges may affect digital feed-through and distortion performance.

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$ set to approximately half the digital positive supply

Figure 18 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar, except that it contains an active pull-down circuit, thus ensuring that the 3PD5651E remains enabled if this input is left disconnected. The internal digital circuitry of the 3PD5651E is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when VDD is set to accommodate the maximum high level voltage, $V_{OH(MAX)}$, of the TTL drivers. A VDD of 3 V to 3.3 V will typically ensure upper compatibility of most TTL logic families.

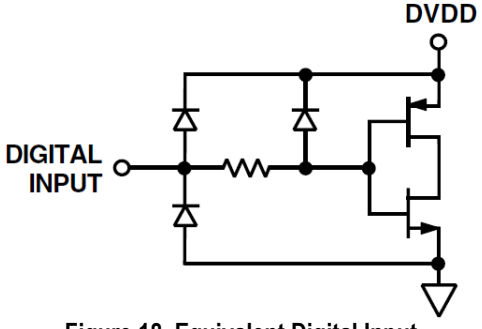


Figure 18. Equivalent Digital Input

Since the 3PD5651E is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the

optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup-and-hold times of the 3PD5651E as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the above conditions will result in the lowest data feed-through and noise. Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20Ω to 100Ω) between the 3PD5651E digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feed-through. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs. Also, operating the 3PD5651E with reduced logic swings and a corresponding digital supply will also reduce data feed-through. The external clock driver circuitry should provide the 3PD5651E with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. However, the clock input could also be driven by via a sine wave, which is centered around the digital threshold (i.e., VDD/2), and meets the min/max logic threshold. This may result in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. Note, at higher sampling rates the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and subsequently cut into the required data setup-and-hold times.

SLEEP MODE OPERATION

The 3PD5651E has a power-down function that turns off the output current and reduces the supply current to less than 8.5mA over the specified supply range of 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level "1" to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures the 3PD5651E remains enabled if this input is left disconnected. The SLEEP input with active pull-down requires <40μA of drive current.

The power-up and power-down characteristics of the 3PD5651E are dependent on the value of the compensation capacitor connected to COMP2 (Pin 23). With a nominal value of 0.1μF, the 3PD5651E takes less than 5μs to power down and approximately 3.25ms to power back up.

POWER DISSIPATION

The power dissipation, P_D, of the 3PD5651E is dependent on several factors, including:
(1) AVDD, the power supply voltages;
(2) I_{OUTFS}, the full-scale current output;
(3) f_{CLOCK}, the update rate;
(4) the reconstructed digital input waveform.

POWER AND GROUNDING CONSIDERATIONS

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection placement and routing and supply bypassing and grounding. The evaluation board for the 3PD5651E, which uses a four layer PCB, serves as a good example for the above mentioned considerations. The evaluation board provides an illustration of the recommended printed circuit board ground, power and signal plane layouts.

Proper grounding and decoupling should be a primary objective in any high speed system. The 3PD5651E features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible.

For those applications requiring a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 22. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

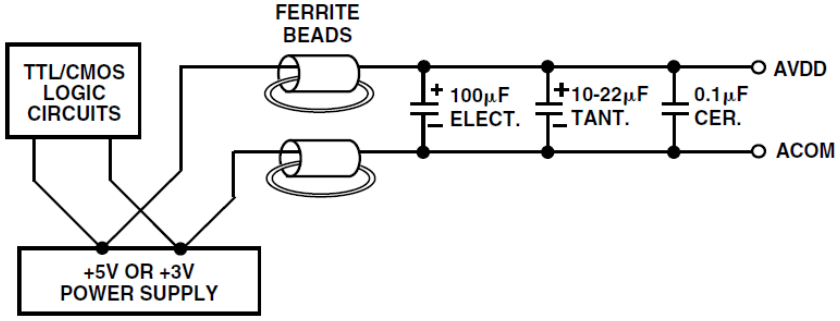


Figure 22. Differential LC Filter for Single +5V or +3V Applications

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the 3PD5651E. If properly implemented,

ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components, should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistor should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For applications requiring the optimum dynamic performance and/or a bipolar output swing, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration is well suited for ac coupling applications. It provides the optimum high frequency performance due to its excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load (i.e., assuming no source termination). The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting.

Figure 23 shows the 3PD5651E in a typical transformer coupled output configuration. The center-tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained within the specified output compliance range of the 3PD5651E. A differential resistor, R_{DIFF}, may be inserted in applications in which the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination. Note that approximately half the signal power will be dissipated across R_{DIFF}.

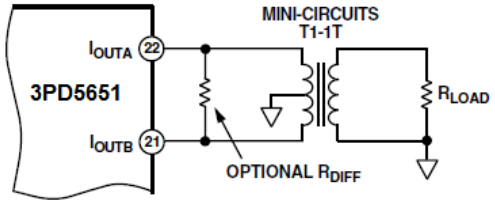


Figure23. Differential Output Using a Transformer

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 24. The 3PD5651E is configured with two equal load resistors, R_{LOAD}, of 25Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB} forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

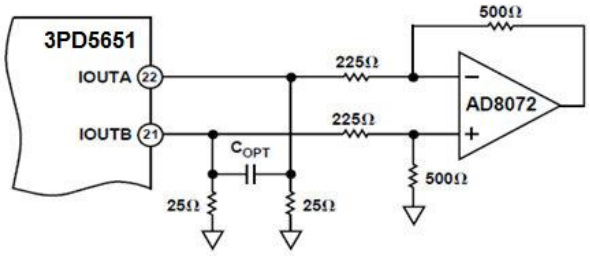


Figure 24. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit is configured to provide some additional signal gain. The op amp must operate off a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the 3PD5651E while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 25 provides the necessary level-shifting required in a single supply system. In this case, AVDD, which is the positive analog supply for both the 3PD5651E and the op amp, is also used to level-shift the differential output of the 3PD5651E to mid-supply (i.e., AVDD/2).

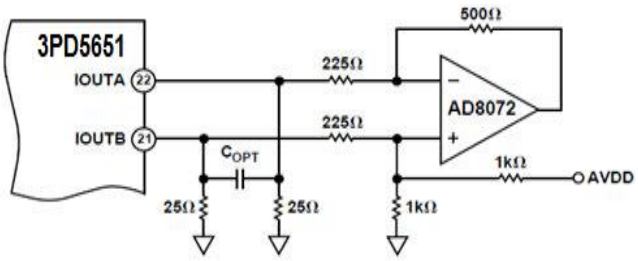
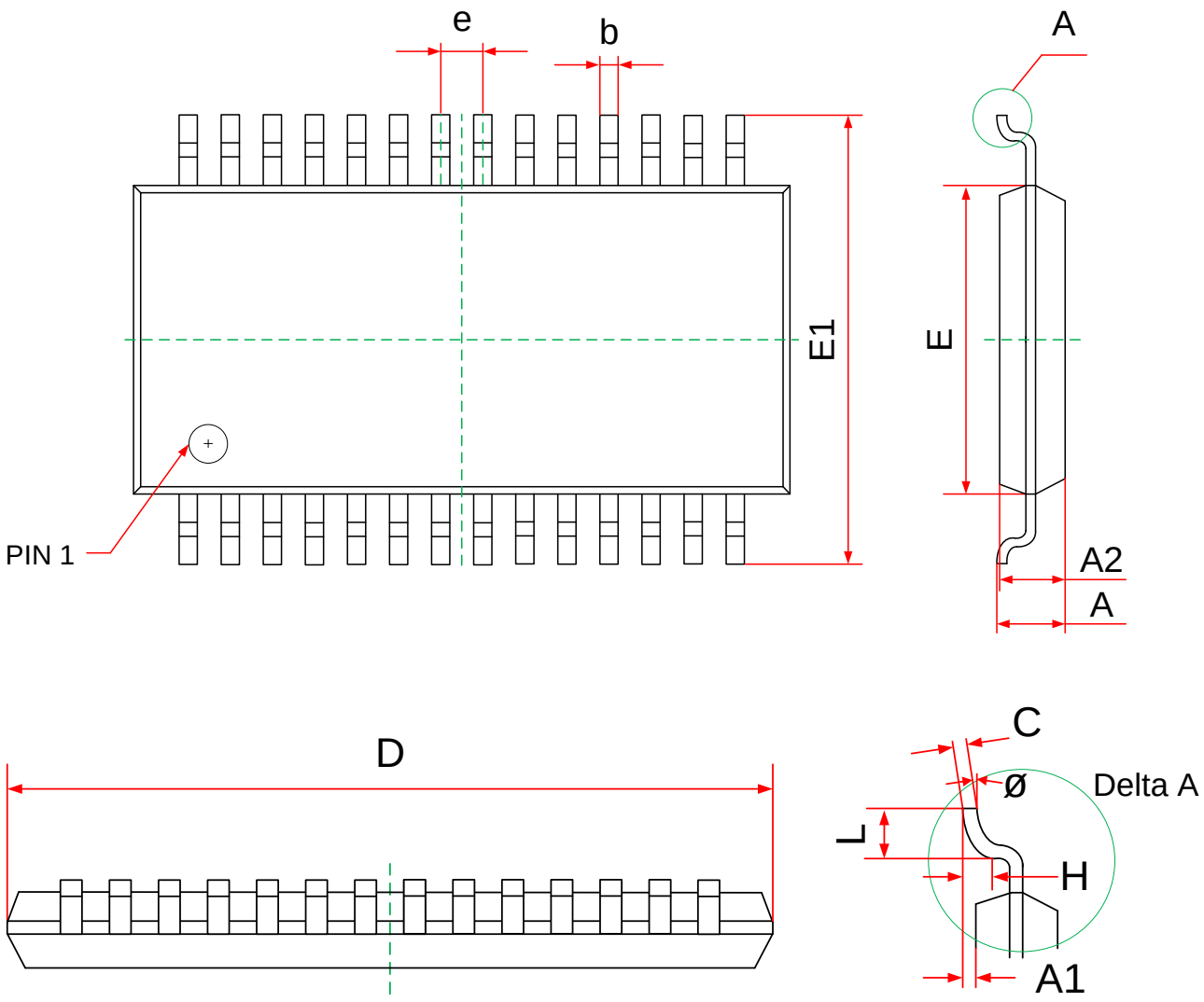


Figure 25. Single-Supply DC Differential Coupled Circuit

OUTLINE DIMENSIONS

28-Lead Thin Shrink Small Outline Package (TSSOP) --Dimensions are shown in millimeters and inches.



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

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