# Octal 16-/12-Bit, Low Power, High Performance DACs

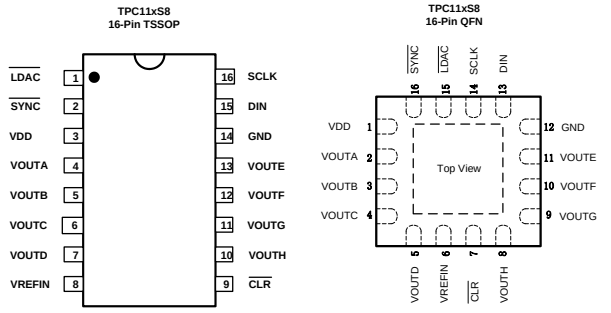
## Features

- **Octal, 16-/12-Bit Pin Compatible DACs**
  **TPC116S8: 16bit**
  **TPC112S8: 12bit**
- **Low Power Consumption (1.6 mA typ)**
- **Differential Nonlinearity: ±1LSB(max)**
- **Glitch Energy: 2nV-s**
- **Power-On Reset to Zero**
- **Supply Range: 2.7V to 5.5V**
- **Buffered Rail-to-Rail Output Operation**
- **Safe Power-On Reset (POR) to Zero DAC Output**
- **Fast 30MHz, 3-Wire, SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- **SYNC Interrupt Facility**
- **Available in QFN16 and TSSOP-16 Package**

## Applications

- Gain and Offset Adjustment
- Process Control and Servo Loops
- Programmable voltage and current sources
- Programmable attenuators
- Automatic Test Equipment

## Package Information (Top View)




## Description

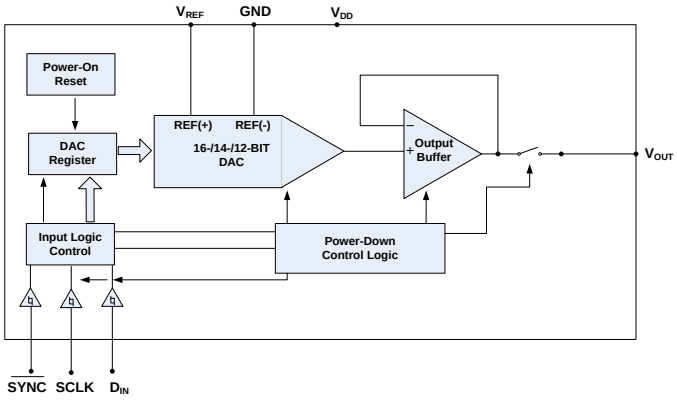
The TPC116S8/TPC112S8 are pin compatible 16-bit and 12-bit digital-to-analog converter, these series product are eight channels, low power, buffered voltage-out DACs and are guaranteed monotonic by design. The devices use a precision external reference applied through the high resistance input for rail-to-rail operation and low system power consumption.

The TPC116S8/ TPC112S8 accepts a wide 2.7V to 5.5V supply voltage range. The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V and remains there until a valid write takes place.

The TPC116S8/ TPC112S8 on-chip precision output amplifier allows rail-to-rail output swing to be achieved. For remote sensing applications, the output amplifier's inverting input is available to the user. The TPC116S8/ TPC112S8 use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The TPC116S8/ TPC112S8 are available in a small size 16-pin TSSOP package, all package are specified over the -40°C to +125°C extended industrial temperature range.






Block diagram of one DAC

## Order Information

| Model Name | Order Number | Package | Transport Media, Quantity | Marking Information |
|---|---|---|---|---|
| TPC112S8 | TPC112S8-TR | 16-Pin TSSOP | Tape and Reel, 3,000 | 112S8 |

| | | | | |
|---|---|---|---|---|
| TPC116S8 | TPC116S8-TR | 16-Pin TSSOP | Tape and Reel, 3,000 | 116S8 |
| TPC116S8 | TPC116S8-QR | 16-Pin QFN | Tape and Reel, 3,000 | 116S8 |

## Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^-$ Note 2.....7.0V
Input Voltage..... $V^-$ – 0.3 to $V^+$ + 0.3
Input Current: +IN, –IN Note 3..... ±20mA
Output Short-Circuit Duration Note 4..... Indefinite
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The supplies must be established simultaneously, with, or before, the application of any input signals.

**Note 3:** The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

**Note 4**: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

## ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|---|---|---|---|---|
| HBM | Human Body Model ESD | ANSI/ESDA/JEDEC JS-001 | 8 | kV |
| CDM | Charged Device Model ESD | ANSI/ESDA/JEDEC JS-002 | 2 | kV |

## Thermal Resistance

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 16-Pin TSSOP | 180 | 35 | °C/W |

## Electrical Characteristics

**($V_{DD}$ = 5V, $V_{REF}$ = 5V, $C_L$ = 100pF, $R_L$ = 10kΩ, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.)**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC ACCURACY (Note 5)** | | | | | | |
| N | Resolution | TPC112S8 | 12 | | | Bits |
| | | TPC116S8 | 16 | | | |
| INL | Integral Nonlinearity | TPC112S8 (12-bit) (Note 6) | -1 | ±0.25 | 1 | LSB |
| | | TPC116S8 (16-bit) (Note 6) | -16 | ±8 | 16 | |
| DNL | Differential Nonlinearity | TPC112S8 (12-bit) (Note 6) | -1 | ±0.05 | 1 | LSB |
| | | TPC116S8 (16-bit) (Note 6) | -1 | ±0.5 | 1 | |
| OE | Zero Offset Error | | | 6.5 | 30 | mV |
| | Full-Scale Offset Error | | -30 | 0 | 30 | mV |
| | Offset-Error Drift | | | ±1 | | μV/°C |
| GE | Gain Error | | -0.3 | ±0.13 | 0.3 | %FS |
| | Gain Temperature Coefficient | | | ±2 | | ppmFS/°C |
| **REFERENCE INPUT** | | | | | | |
| $V_{REF}$ | Reference-Input Voltage Range | | 0.5 | | $V_{DD}$ | V |
| $R_{REF}$ | Reference-Input Impedance | | | 333 | | kΩ |
| **DAC OUTPUT** | | | | | | |
| | Output Voltage Range | No load (typical) | | | $V_{REF}$ | V |
| | | 10 kΩ load | 0.2 | | $V_{REF}$-0.1 | |
| | DC Output Impedance | | | 0.1 | | Ω |
| $C_L$ | Capacitive Load (Note 7) | Series resistance = 0Ω | | | 0.1 | nF |
| | | Series resistance = 1kΩ | | | 15 | μF |
| $R_L$ | Resistive Load (Note 7) | | 5 | | | kΩ |
| | Short-Circuit Current | $V_{DD}$ = 5.5V | | 35 | | mA |
| | Power-Up Time | From power-down mode | | 25 | | μs |
| **DIGITAL INPUTS (SCLK, DIN, $\overline{SYNC}$)** | | | | | | |
| $V_{IH}$ | Input High Voltage | $V_{DD}$ = 5V | 2 | | | V |
| | | $V_{DD}$ = 3.3V | 1.5 | | | V |
| $V_{IL}$ | Input Low Voltage | $V_{DD}$ = 5V | | | 0.6 | V |
| | | $V_{DD}$ = 3.3V | | | 0.4 | V |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 0V or $V_{DD}$ | | ±5 | ±10 | μA |
| $C_{IN}$ | Input Capacitance | | | 1 | | pF |

## Electrical Characteristics(continued)

**($V_{DD}$ = 5V, $V_{REF}$ = 5V, $C_L$ = 100pF, $R_L$ = 10kΩ, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{HYS}$ | Hysteresis Voltage | | | 0.15 | | V |
| **DYNAMIC PERFORMANCE (Note 7)** | | | | | | |
| SR | Voltage-Output Slew Rate | Positive and negative | | 1 | | V/μs |
| BW | Voltage-Output Settling Time | 1/4 scale to 3/4 scale, to ⩽ 0.5 LSB, 12-bit | | 14 | | μs |
| | Reference -3dB Bandwidth | Hex code = 800 (TPC112S8),<br>Hex code = 8000 (TPC116S8) | | 100 | | kHz |
| | Digital Feedthrough | Code = 0, all digital inputs from 0V to VDD, SCLK < 50MHz | | 0.5 | | nV • s |
| | DAC Glitch Impulse | Major code transition | | 2 | | nV • s |
| | Output Noise | 10kHz | | 90 | | nV/ √ Hz |
| | Integrated Output Noise | 0.1Hz to 10Hz | | 25 | | $\mu V_{P-P}$ |
| **POWER REQUIREMENTS** | | | | | | |
| $V_{DD}$ | Supply Voltage | | 2.7 | | 5.5 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$ = 5V , No load; all digital inputs at 0V or $V_{DD}$, supply current only; excludes reference input current, midscale | | 0.8 | 1.5 | mA |
| $I_{DD}$ | Supply Current | $V_{DD}$ = 3.3V , No load; all digital inputs at 0V or $V_{DD}$, supply current only; excludes reference input current, midscale | | 0.5 | 1 | mA |
| | Power-Down Supply Current | No load, all digital inputs at 0V or $V_{DD}$ | | | 500 | μA |

**Note 5:** Linearity is tested within 20mV of GND and $V_{DD}$.

**Note 6:** Gain and offset is tested within 100mV of GND and $V_{DD}$.

**Note 7:** All timing specifications measured with $V_{IL} = V_{GND}$, $V_{IH} = V_{DD}$.

## Serial Write Operation

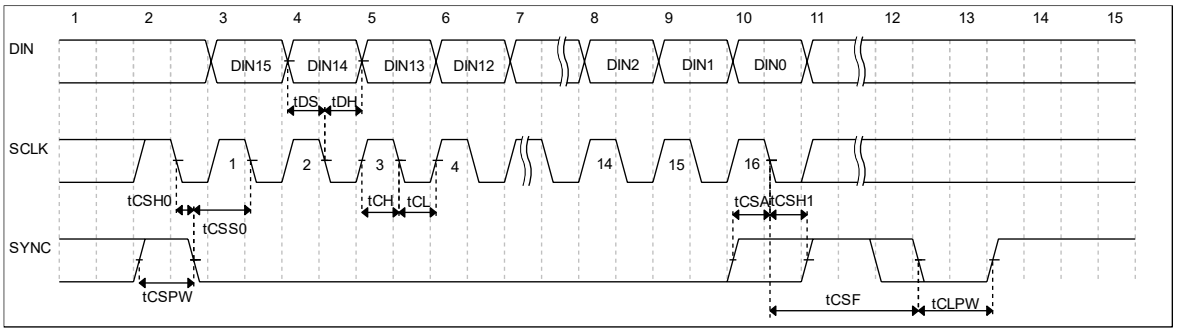



**Figure 1. 16-Bit Serial-Interface Timing Diagram (TPC112S8)**

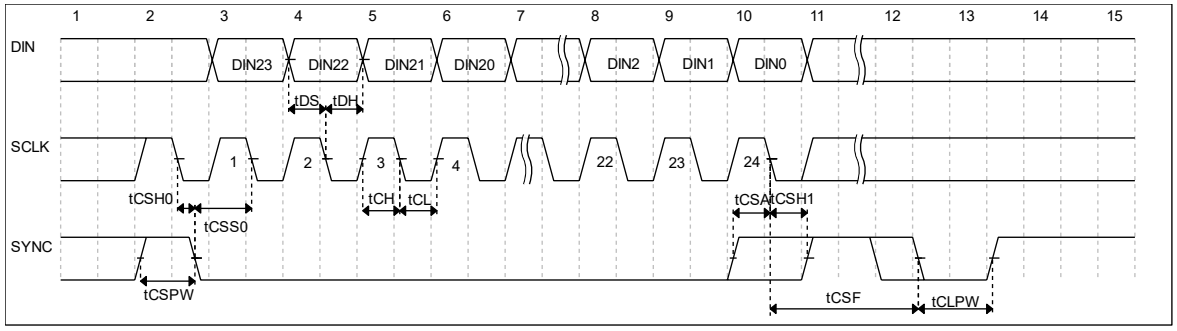



**Figure 2. 24-Bit Serial-Interface Timing Diagram (TPC116S8)**

**TIMING CHARACTERISTICS (Figures 1,2 and 3)**

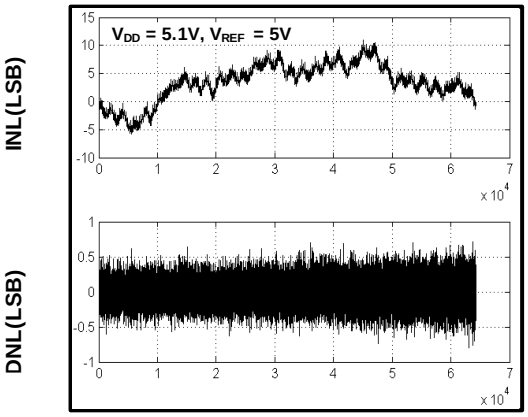
| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $f_{SCLK}$ | Serial Clock Frequency | | 0 | | 30 | MHz |
| $t_{CH}$ | SCLK Pulse-Width High | | 8 | | | ns |
| $t_{CL}$ | SCLK Pulse-Width Low | | 8 | | | ns |
| $t_{CSS0}$ | $\overline{SYNC}$ Fall to SCLK Fall Setup Time | | 8 | | | ns |
| $t_{CSH0}$ | $\overline{SYNC}$ Fall to SCLK Fall Hold Time | | 0 | | | ns |
| $t_{CSH1}$ | $\overline{SYNC}$ Rise to SCLK Fall Hold Time | | 0 | | | ns |
| $t_{CSA}$ | $\overline{SYNC}$ Rise to SCLK Fall | | 12 | | | ns |
| $t_{CSF}$ | SCLK Fall to $\overline{SYNC}$ Fall | | 100 | | | ns |
| $t_{DS}$ | DIN to SCLK Fall Setup Time | | 5 | | | ns |
| $t_{DH}$ | DIN to SCLK Fall Hold Time | | 4.5 | | | ns |
| $t_{CSPW}$ | $\overline{SYNC}$ Pulse-Width High | | 20 | | | ns |
| $t_{CLPW}$ | $\overline{SYNC}$ Pulse-Width Low | | 20 | | | ns |

**Note:** Parameters are provided by lab bench test and design simulation

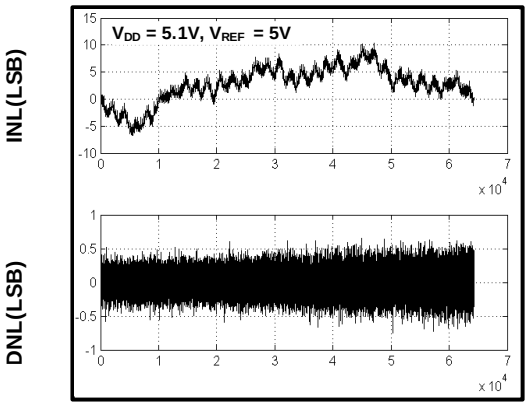
## Typical Performance Characteristics

$V_S$ = 5V, At $T_A$ = +25°C, unless otherwise specified

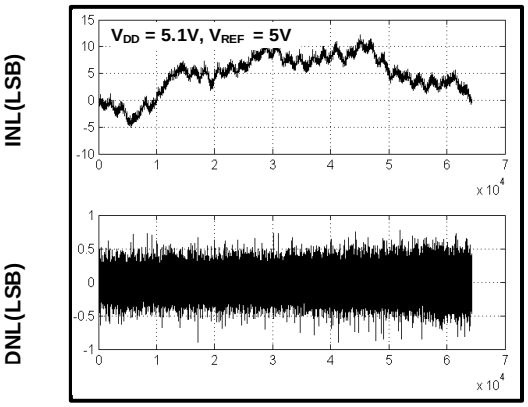
**INL and DNL vs. Digital Input Code(+25°C TPC116S8)**




**INL and DNL vs. Digital Input Code(-40°C TPC116S8)**



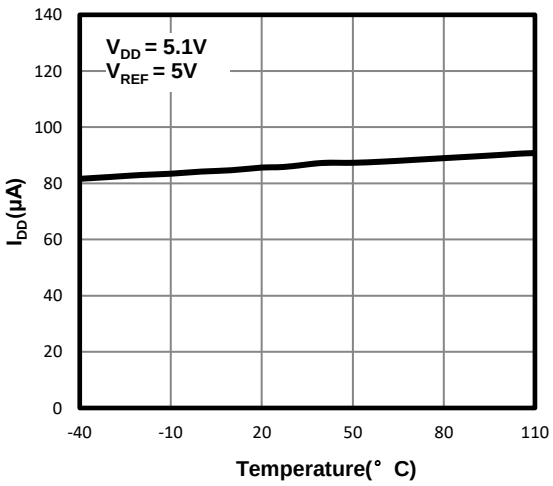

**INL and DNL vs. Digital Input Code(+105°C TPC116S8)**



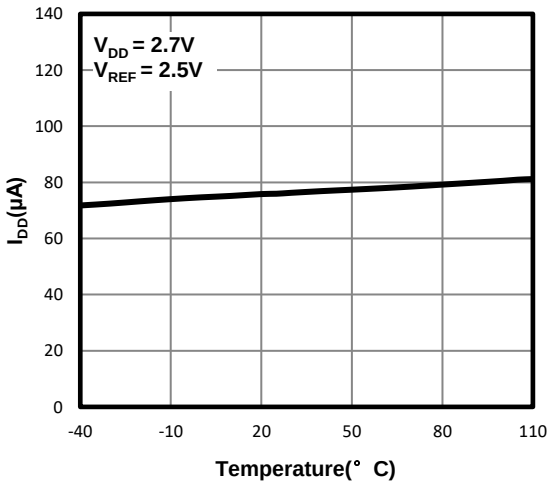
## Typical Performance Characteristics

$V_S$ = 5V, At $T_A$ = +25°C, unless otherwise specified

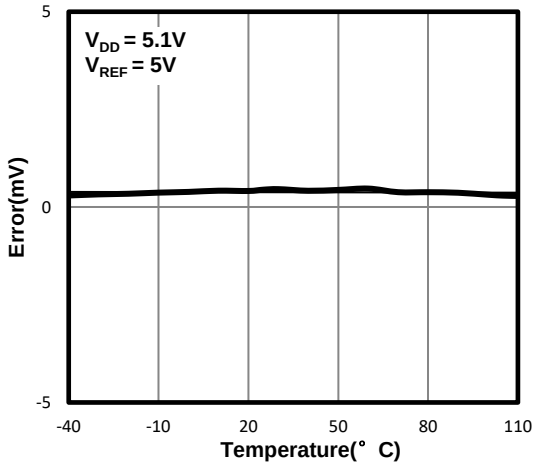
**Power-Supply Current vs. Temperature(TPC116S8)**



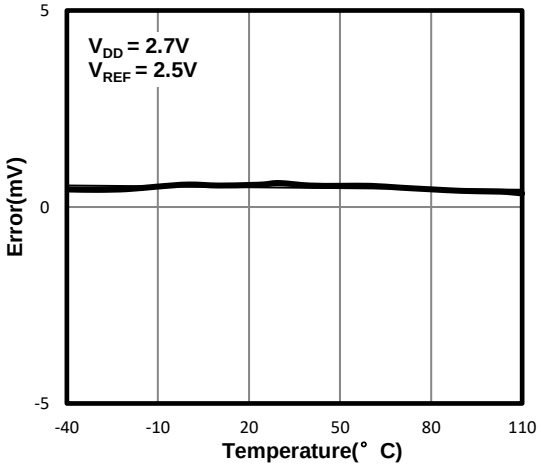

**Power-Supply Current vs. Temperature(TPC116S8)**




**Zero-Scale Error vs. Temperature(TPC116S8)**

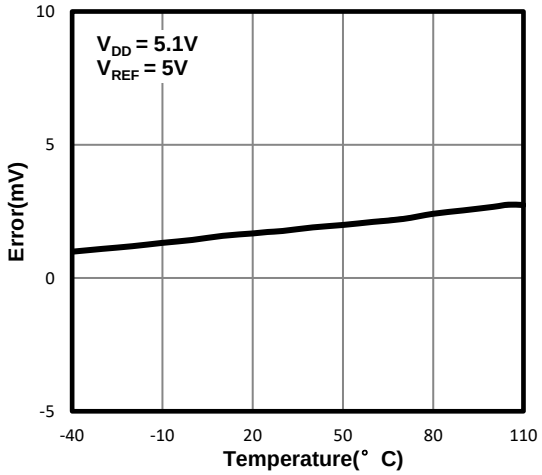


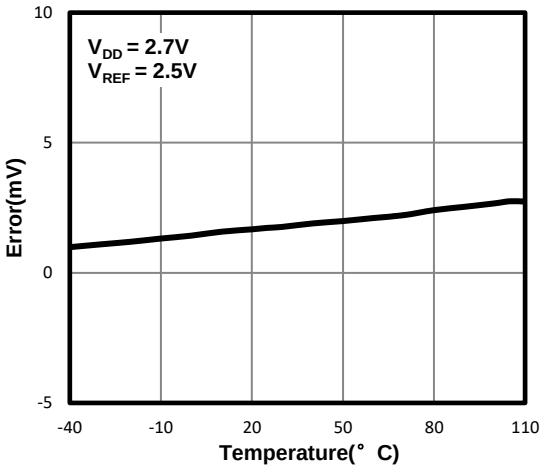

**Zero-Scale Error vs. Temperature(TPC116S8)**




**Full-Scale Error vs. Temperature(TPC116S8)**

**Full-Scale Error vs. Temperature(TPC116S8)**

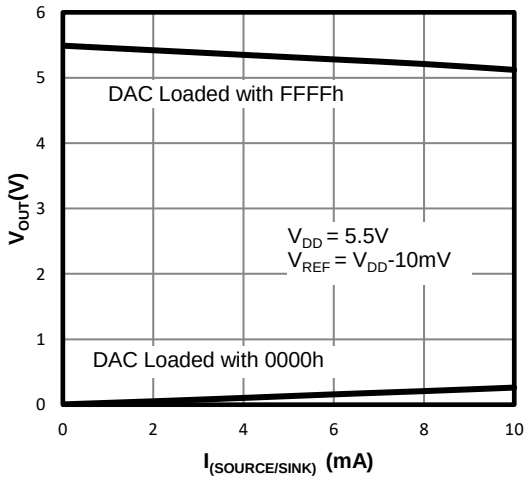


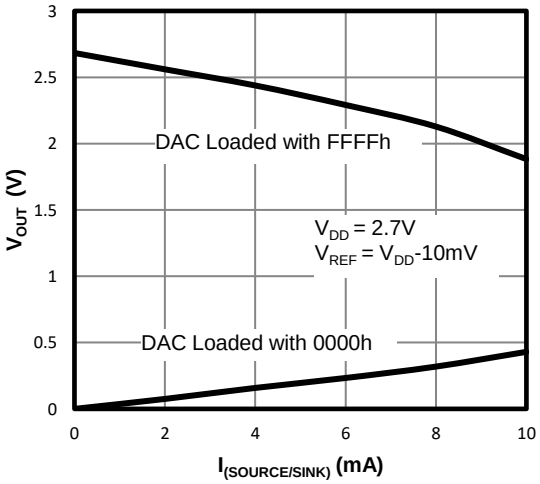

## Typical Performance Characteristics

$V_S$ = 5V, At $T_A$ = +25°C, unless otherwise specified

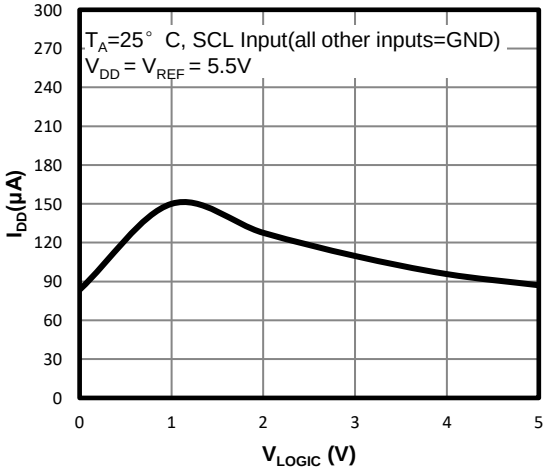
**Source and Sink Current Capability(TPC116S8)**



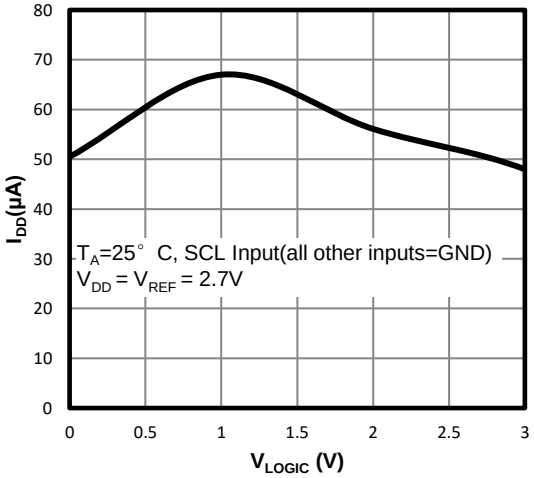

**Source and Sink Current Capability(TPC116S8)**



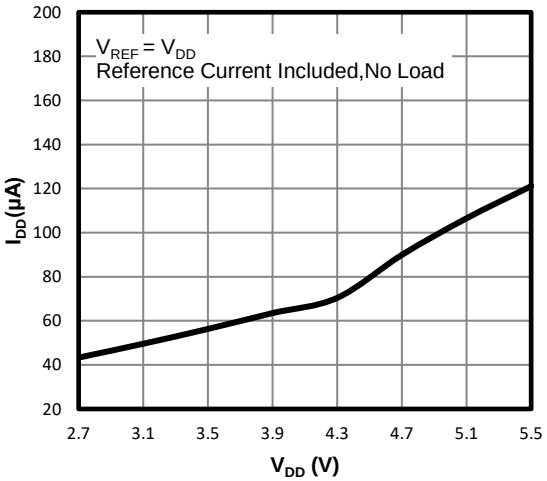

**Supply Current vs. Logic Input Voltage(TPC116S8)**



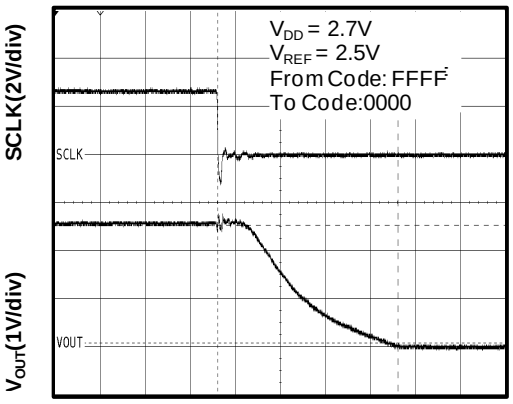

**Supply Current vs. Logic Input Voltage(TPC116S8)**



**Supply Current vs. Supply Voltage(TPC116S8)**




**Full-Scale Settling Time(2.7V Falling Edge)**

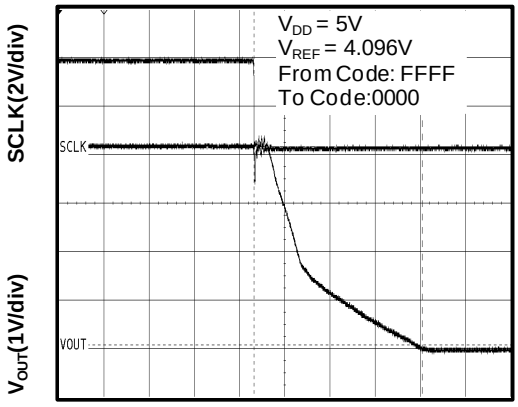



**Time (160ns/div)**

## Typical Performance Characteristics

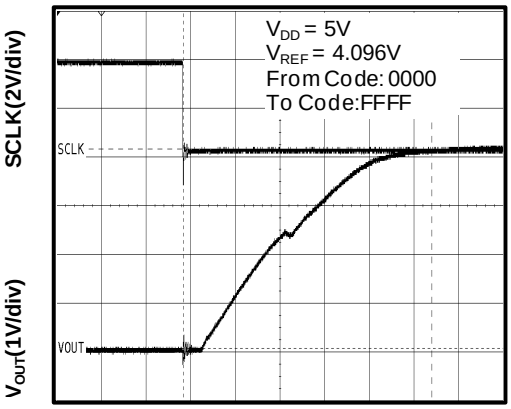
$V_S$ = 5V, At $T_A$ = +25°C, unless otherwise specified

**Full-Scale Settling Time(5V Falling Edge)**



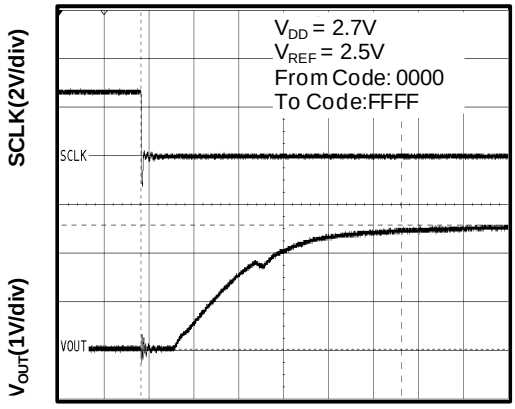

**Time (250ns/div)**

**Full-Scale Settling Time(5V Rising Edge)**




**Time (500ns/div)**

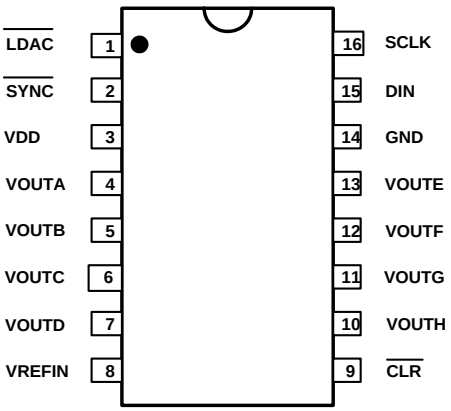
**Full-Scale Settling Time(2.7V Rising Edge)**



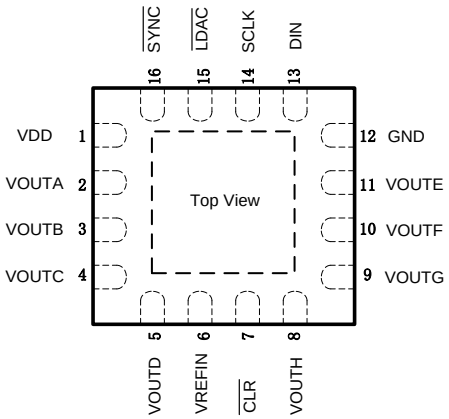

Time (430ns/div)

## Pin Functions

TPC11xS8
16-Pin TSSOP




TPC11xS8
16-Pin QFN



| PIN Name | TSSOP PIN number | QFN PIN number | Function |
|---|---|---|---|
| $\overline{\text{LDAC}}$ | 1 | 15 | Load DAC. When the LOAD signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is low. |
| $\overline{\text{SYNC}}$ | 2 | 16 | Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. |
| VDD | 3 | 1 | Power supply input, 2.7V to 5.5V |
| OUTA | 4 | 2 | DACA output |
| OUTB | 5 | 3 | DACB output |
| OUTC | 6 | 4 | DACC output |
| OUTD | 7 | 5 | DACD output |
| VREFIN | 8 | 6 | Reference voltage input |
| $\overline{\text{CLR}}$ | 9 | 7 | Active Low. When it goes low, the DAC register is cleared and DAC output is reset to zero. |
| OUTH | 10 | 8 | DACH output |
| OUTG | 11 | 9 | DACG output |
| OUTF | 12 | 10 | DACF output |
| OUTE | 13 | 11 | DACE output |
| GND | 14 | 12 | Ground reference point for all circuitry on the part. |
| DIN | 15 | 13 | Serial data input. Data is clocked into the 16-/24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input. |
| SCLK | 16 | 14 | Serial clock input. Data can be transferred at rates up to 30MHz. Schmitt-Trigger logic input. |
| Thermal PAD | | Thermal PAD | Connected to GND internally. Suggest to connect it to GND. |

# Detailed Description

The TPC116S8/TPC112S8 are pin-compatible and software-compatible 12-bit and 16-bit DACs. The TPC116S8/TPC112S8 are 4-channels, low-power, high-reference input resistance, and buffered voltage-output DACs. The TPC116S8/TPC112S8 minimize the digital noise feed through from their inputs to their outputs by powering down the SCLK and DIN input buffers after completion of each data frame. The data frames are 16-bit for the TPC112S8 and 24-bit for the TPC116S8. On power-up, the TPC116S8/TPC112S8 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The TPC116S8/ TPC112S8 contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, power-on-reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

# Applications Information

## DAC Reference (REF)

The external reference input features a typical input impedance of 333kΩ and accepts an input voltage from +2V to VDD. Connect an external voltage supply between REF and GND to apply an external reference.

## Serial Interface

The TPC116S8/TPC112S8 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK, SYNC, and DIN. The chip-select input (SYNC) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16-bit for the TPC112S8 and 24-bit for the TPC116S8. The first 3 bits are the control bits followed by 1 power-down bit as well as 12 data bits (MSB first) for the TPC112S8 and 22 data bits (MSB first) for the TPC116S8 as shown in Tables 1 and 2. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer, drive SYNC high and keep SYNC high for a minimum of 20ns before the next write sequence. The SCLK can be either high or low between SYNC write pulses. Figures 1 and 2 show the timing diagram for the complete 3-wire serial interface transmission. The TPC116S8 DAC code is unipolar binary with VOUT = (code/65,536) x VREF. The TPC112S8 DAC code is unipolar binary with VOUT = (code/4096) x VREF.

**Table 1. Operating Mode Truth Table (TPC112S8)**

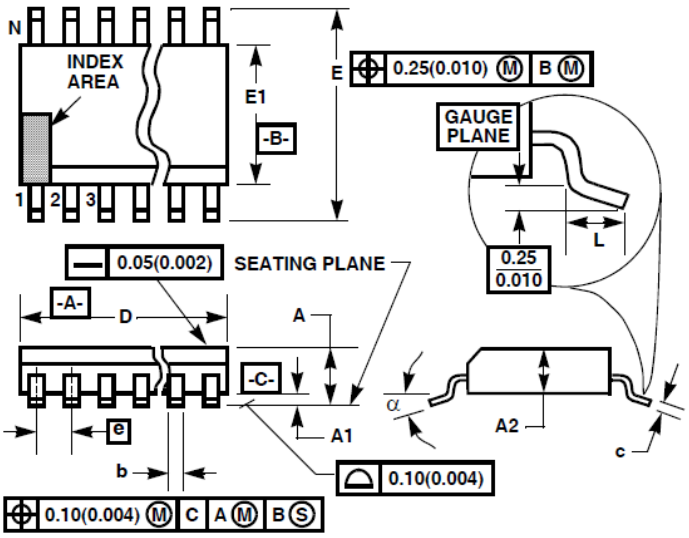
| 16-BIT WORD | | | | | Function |
|---|---|---|---|---|---|
| A2 | A1 | A0 | PD | DAC Data Bit | |
| D15 | D14 | D13 | D12 | D11～D0 | |
| 0 | 0 | 0 | 0 | X | Update DAC A Data |
| 0 | 0 | 1 | 0 | X | Update DAC B Data |
| 0 | 1 | 0 | 0 | X | Update DAC C Data |
| 0 | 1 | 1 | 0 | X | Update DAC D Data |
| 1 | 0 | 0 | 0 | X | Update DAC E Data |
| 1 | 0 | 1 | 0 | X | Update DAC F Data |
| 1 | 1 | 0 | 0 | X | Update DAC G Data |
| 1 | 1 | 1 | 0 | X | Update DAC H Data |
| X | X | X | 1 | X | Power down (output High Z) |

**Table 2. Operating Mode Truth Table (TPC116S8)**

| 24-BIT WORD | | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|
| MSB ( No content) | | | | A2 | A1 | A0 | PD | DAC Data Bit | |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15～D0 | |
| X | X | X | X | 0 | 0 | 0 | 0 | X | Update DAC A Data |
| X | X | X | X | 0 | 0 | 1 | 0 | X | Update DAC B Data |
| X | X | X | X | 0 | 1 | 0 | 0 | X | Update DAC C Data |
| X | X | X | X | 0 | 1 | 1 | 0 | X | Update DAC D Data |
| X | X | X | X | 1 | 0 | 0 | 0 | X | Update DAC E Data |
| X | X | X | X | 1 | 0 | 1 | 0 | X | Update DAC F Data |
| X | X | X | X | 1 | 1 | 0 | 0 | X | Update DAC G Data |
| X | X | X | X | 1 | 1 | 1 | 0 | X | Update DAC H Data |
| X | X | X | X | X | X | X | 1 | X | Power down (output High Z) |

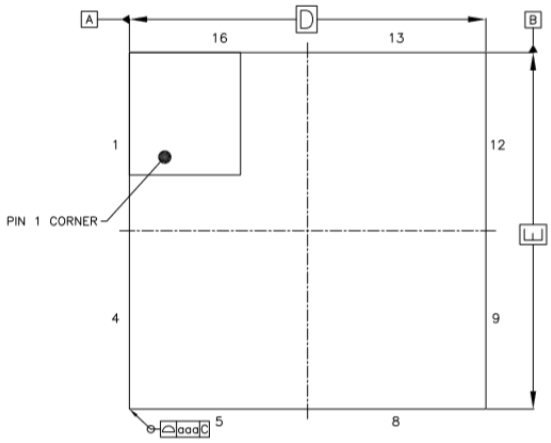
## Package Outline Dimensions

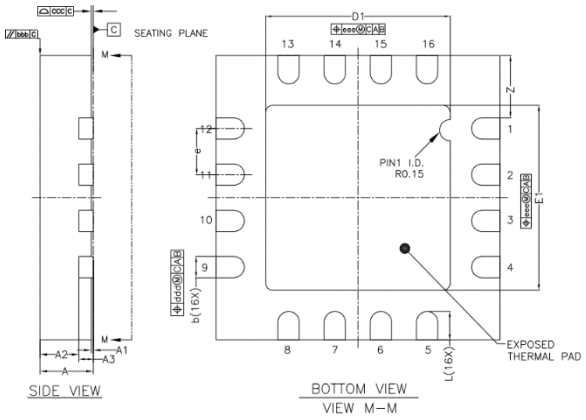
**TSSOP-16**




| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 0.55 | 1.10 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.90 | 0.95 |
| b | 0.19 | 0.25 | 0.30 |
| c | 0.09 | 0.15 | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.25 | 6.38 | 6.5 |
| L | 0.50 | 0.60 | 0.70 |
| N | 16 | | |
| e | 0.65 BSC | | |
| α | 0° | 4° | 8° |

## QFN4x4-16L




TOP VIEW

| DESCRIPTION | | SYMBOL | MILLIMETER | | |
|---|---|---|---|---|---|
| | | | MIN | NOM | MAX |
| TOTAL THICKNESS | | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | | A1 | 0.00 | -- | 0.05 |
| MOLD THICKNESS | | A2 | 0.50 | 0.55 | 0.60 |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| BODY SIZE | X | D | 3.90 | 4.00 | 4.10 |
| | Y | E | 3.90 | 4.00 | 4.10 |
| LEAD PITCH | | e | 0.65 BSC | | |
| LEAD WIDTH | | b | 0.25 | 0.30 | 0.35 |
| LEAD LENGTH | | L | 0.35 | 0.40 | 0.45 |
| EP SIZE | | D1 | 2.55 | 2.60 | 2.65 |
| | | E1 | 2.55 | 2.60 | 2.65 |
| LEAD EDGE TO PKG EDGE | | Z | 0.875 BSC | | |
| Tolerance of form and position | | | | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| LEAD COPLANARITY | | ccc | 0.08 | | |
| LEAD POSITION OFFSET | | ddd | 0.1 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

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