

## Features

- 1-FHDTV Video Filter Support FHD CVI-1080p60
- 1-HDTV Video Filter Support HD CVI-1080p30/720p60
- Optimized 6th-order Butterworth Video reconstruction filter:
  - FHD Channel:  $-3 \text{ dB} \geq 72 \text{ MHz}$
  - HD Channel:  $-3 \text{ dB} \geq 36 \text{ MHz}$
- Support Multiple Input Biasing:
  - Provide 80-mV Level-Shift when DC-Coupled
- Transparent Input Clamping when AC-Coupled
- Support External DC Biasing when AC-Coupled
- Very Low Quiescent Current: 6/11.5 mA (at 3.3 V, HD/FHD typ.)
- 6 dB Gain (2 V/V), Rail to Rail Output
- AC- or DC-Coupled Output Driving Dual Video Loads (75  $\Omega$ )
- Wide Power Supply: +3.0 V to +5.5 V Single Supply
- Robust ESD Protection: Robust 8 kV – HBM and 2 kV – CDM ESD Rating
- Green Product, SOT23-6 Package

## Applications

- Video Signal Amplification
- Set-Top Box Video Driver
- PVR, DVD Player Video Buffer
- Video Buffer for Portable or USB-Powered Video Devices
- HDTV

## Description

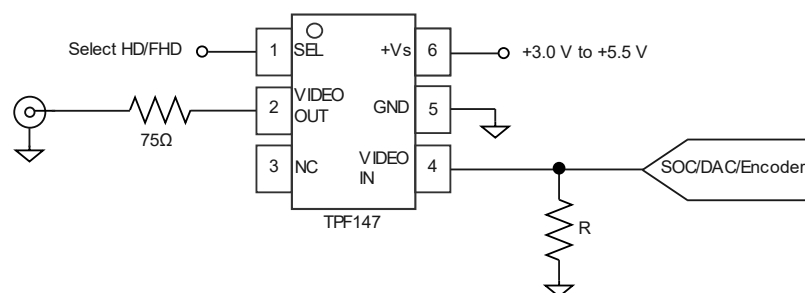
The TPF147 is specially designed for consumer applications, high-performance, low-cost video reconstruction filter, it combines excellent video performance and low power consumption perfectly. It incorporates one selectable full high-definition (FHD) and one high-definition (HD) filter channel. All filters feature sixth-order Butterworth characteristics that are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) anti-aliasing filters. The FHD filters can be bypassed to support 1080p60 video, and the HD filters can be bypassed to support 720p60 or 1080i60 video.

As part of the TP147 flexibility, the input can be configured for ac- or dc-coupled inputs. The 84-mV output level shift allows a full sync dynamic range at the output with 0-V input. The ac-coupled modes include a transparent sync-tip clamp option for composite video (CVI), Y', and G'B'R' signals. AC-coupled biasing for C'/P'B/P'R channels can be easily achieved by adding an external resistor to VS+.

The TP147 rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive two lines, or 75- $\Omega$  loads, allows for the maximum flexibility as a video line driver. The 6/11.5-mA total quiescent current at 3.3 V makes it an excellent choice for power-sensitive video applications.

The TPF147 is available in a SOT23-6 package (TPF147-TR). Its operating temperature range is from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

## Typical Application Circuit



**Single-Supply, DC Coupled Video Line Driver**

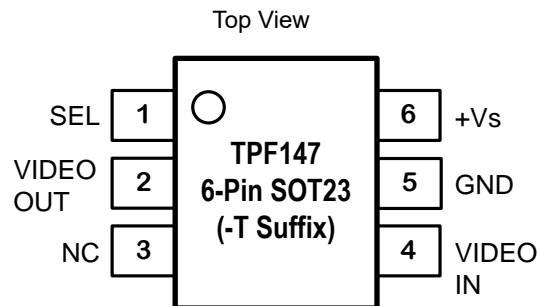
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## Revision History

Date	Revision	Notes
2015-01-10	Rev.A.0	Initial Release
2015-04-13	Rev.A.1	Deleted $V_{IH}$ Max Value data, add $V_{IH}$ Min Value data 1.6 V. Deleted $V_{IL}$ Min Value data, add $V_{IL}$ Max Value data 0.4 V.
2021-12-15	Rev.A.2	Deleted MSOP in Package Outline Dimensions, added SOT23-6 package

### Pin Configuration and Functions



### Pin Functions

Pin		I/O	Description
No.	Name		
1	SEL	I	Select filter 36 MHz or 72 MHz, Logic high select the FHD channel and logic low select the HD channel (when one channel is selected, the other channel is powered down). <b>This pin defaults to logic high if left open.</b>
2	VIDEO OUT	O	Video output
3	NC	-	No Connection
4	VIDEO IN	I	Video input
5	GND	-	Ground
6	+Vs	I	Positive Power Supply

## Specifications

### Absolute Maximum Ratings

Parameter		Min	Max	Unit
+Vs to GND	Power Supply		6	V
V <sub>IN</sub>	Input Voltage	GND - 0.3	V <sub>DD</sub> + 0.3	V
I <sub>O</sub>	Output Current	-65	+65	mA
T <sub>J</sub>	Maximum Junction Temperature	-40	125	°C
T <sub>A</sub>	Operating Temperature Range	-45	85	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
T <sub>L</sub>	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

### ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	8	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

### Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
+Vs	Power Supply	3		5.5	V
T <sub>A</sub>	Operating Temperature Range	-45		85	°C

### Thermal Information

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
SOT23-6	128.9	66.9	°C/W

**Electrical Characteristics**

 All test conditions:  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 150\ \Omega$  to GND, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input Electrical Specifications</b>						
+V <sub>S</sub>	Supply Voltage Range		3.0		5.5	V
I <sub>Q</sub>	Quiescent Current	+V <sub>S</sub> = 3.3 V, V <sub>IN</sub> = 500 mV, no load, select FHD channel		11.5	14.27	mA
		+V <sub>S</sub> = 3.3 V, V <sub>IN</sub> = 500 mV, no load, select HD channel		6	7.44	mA
		+V <sub>S</sub> = 5 V, V <sub>IN</sub> = 500 mV, no load, select FHD channel		15	18.53	mA
		+V <sub>S</sub> = 5 V, V <sub>IN</sub> = 500 mV, no load, select HD channel		7	9.6	mA
I <sub>CLAMP-DOWN</sub>	Clamp Discharge Current	V <sub>IN</sub> = 300 mV, measure current	1.5	2.0	5.1	μA
I <sub>CLAMP-UP</sub>	Clamp Charge Current	V <sub>Y</sub> = -0.2 V	-1.5	-1.7		mA
V <sub>CLAMP</sub>	Input Voltage Clamp	I <sub>Y</sub> = -100 μA	-40	0	+40	mV
R <sub>IN</sub>	Input Impedance	0.5 V < V <sub>Y</sub> < 1 V	0.5	3		MΩ
AV	Voltage Gain	V <sub>IN</sub> = 0.5 V, 1 V or 2 V R <sub>L</sub> = 150 Ω to GND	5.9	6.01	6.03	dB
ΔAV	Channel Mismatch		-2		+2	%
V <sub>OLS</sub>	Output Level Shift Voltage	V <sub>IN</sub> = 0 V, no load, input referred	53	80	124	mV
V <sub>OL</sub>	Output Voltage Low Swing	V <sub>IN</sub> = -0.3 V, R <sub>L</sub> = 75 Ω		0.05		V
V <sub>OH</sub>	Output Voltage High Swing	V <sub>IN</sub> = 3V, R <sub>L</sub> = 75 Ω to GND (dual load)		3.18		V
PSRR	Power Supply Rejection Ratio	ΔV <sub>DD</sub> = 3.3 V to 3.6 V		61		dB
		ΔV <sub>DD</sub> = 5.0 V to 5.5 V, 50 Hz		67		dB
I <sub>SC</sub>	Short-circuit Current	V <sub>IN</sub> = 2 V, 10 Ω, output to GND	65			mA
		V <sub>IN</sub> = 0.1 V, output short to V <sub>DD</sub>	65			mA
V <sub>IH</sub>	Select High Voltage Threshold	V <sub>DD</sub> = 3.0 V to 5.5 V	1.6			V
V <sub>IL</sub>	Select Low Voltage Threshold	V <sub>DD</sub> = 3.0 V to 5.5 V			0.4	V
t <sub>ON</sub>	Enable Time	V <sub>IN</sub> = 500 mV, V <sub>OUT</sub> to 1%		1000		ns
t <sub>OFF</sub>	Disable Time	V <sub>IN</sub> = 500 mV, V <sub>OUT</sub> to 1%		1000		ns

**Electrical Characteristics (Continued)**

 All test conditions:  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 150\ \Omega$  to GND, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>AC Electrical Specifications</b>							
$f_{-1dB}$	-1dB Bandwidth	HD Channel	$R_L = 150\ \Omega$	27.3	31	34.7	MHz
		FHD Channel		53.1	63.2	72.9	
$f_{-3dB}$	-3dB Bandwidth	HD Channel	$R_L = 150\ \Omega$	31.9	35.5	39.3	MHz
		FHD Channel		63.7	71.5	80.1	
$Att_{27MHz}$	Stop Band Attenuation	HD Channel	$f = 74.25\text{ MHz}$	32.3	38		dB
		FHD Channel	$f = 148\text{ MHz}$	34.0	39.0		dB
dG	Differential Gain	HD Channel	Video input range 1 V		0.2	0.5	%
		FHD Channel	Video input range 1 V	-0.1	0.4	0.8	%
dP	Differential Phase	HD Channel	Video input range 1 V		0.4	0.6	$^\circ$
		FHD Channel	Video input range 1 V	-1.1	0.7	1.1	$^\circ$
THD	Total Harmonic Distortion	HD Channel	$f = 1\text{ MHz}$ , $V_{OUT} = 1.4V_{PP}$		0.02		%
		FHD Channel	$f = 10\text{ MHz}$ , $V_{OUT} = 1.4V_{PP}$		0.15		
D/DT	Group Delay Variation	HD Channel	$f = 100\text{ kHz to }27\text{ MHz}$		5		ns
		FHD Channel	$f = 100\text{ kHz to }60\text{ MHz}$		6.0		
$X_{TALK}$	Channel Crosstalk		$f = 1\text{ MHz}$ , $V_{OUT} = 1.4V_{PP}$	-68	-74		dB
SNR	Signal-to-Noise Ration	HD Channel	$f = 100\text{ kHz to }30\text{ MHz}$	66	71		dB
		FHD Channel	$f = 100\text{ kHz to }60\text{ MHz}$		64		
$R_{OUT\_AC}$	Output Impedance		$f = 10\text{ MHz}$		0.5		$\Omega$

Typical Performance Characteristics

All test conditions:  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 150\ \Omega$  to GND, unless otherwise noted.

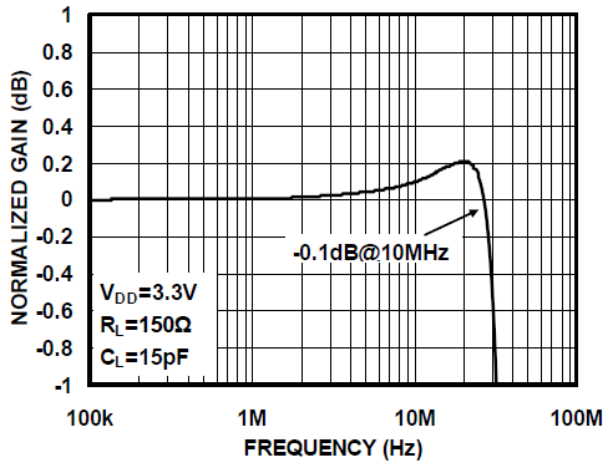


Figure 1 Small-Scale Frequency Response (HD Channel)

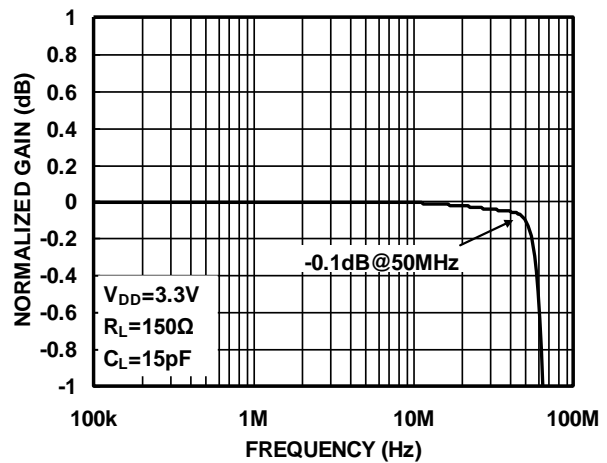


Figure 2 Small-Scale Frequency Response (FHD Channel)

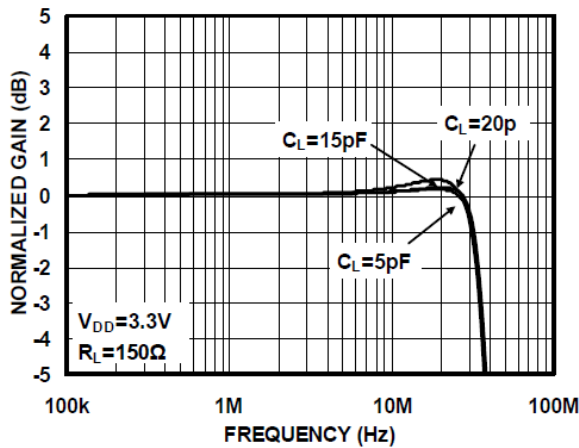


Figure 3 Gain Vs. Frequency with  $C_{LOAD}$  (HD Channel)

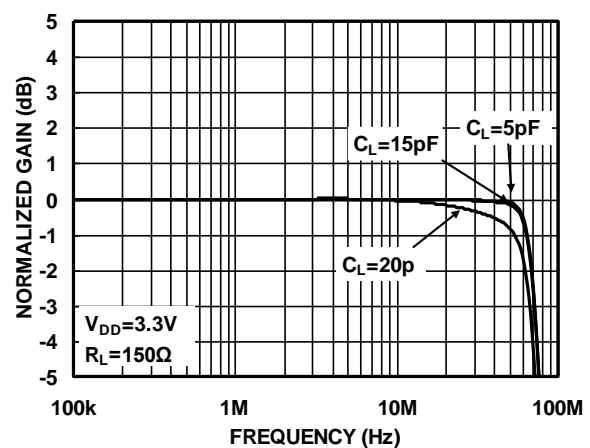


Figure 4 Gain Vs. Frequency with  $C_{LOAD}$  (FHD Channel)

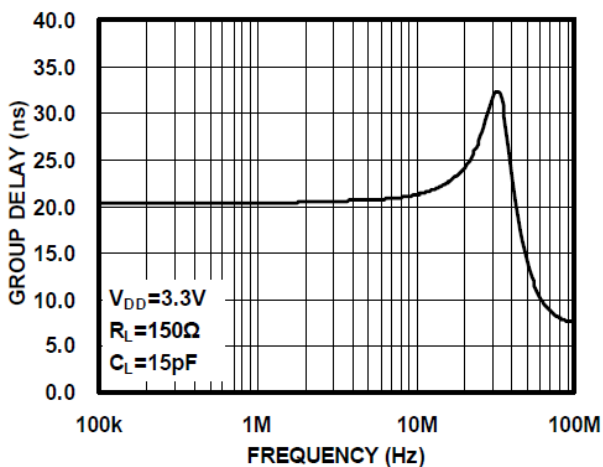


Figure 5 Group Delay vs Frequency (HD Channel)

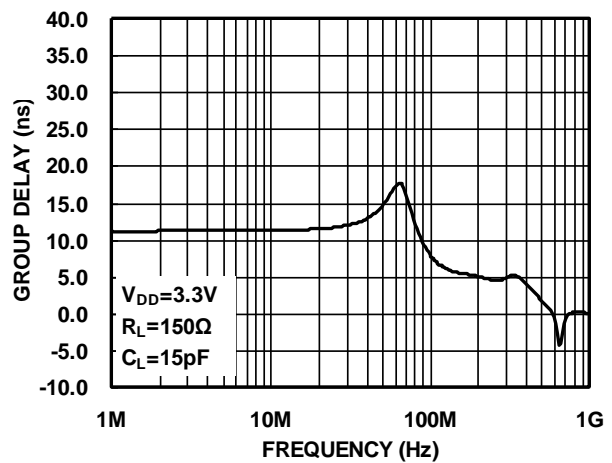


Figure 6 Group Delay vs Frequency (FHD Channel)



Typical Performance Characteristics (Continued)

All test conditions:  $V_{DD} = 3.3\text{ V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 150\ \Omega$  to GND, unless otherwise noted.

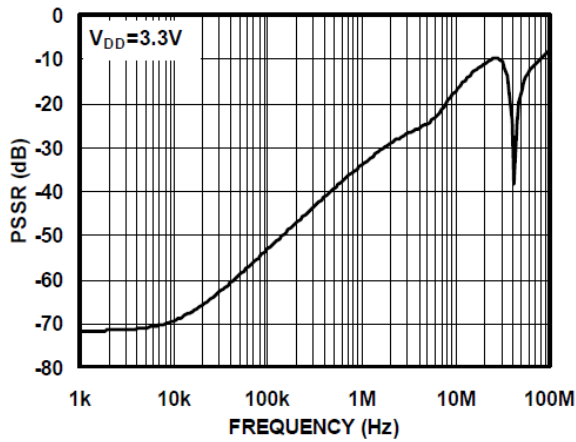


Figure 7 PSRR Vs. Frequency (HD)

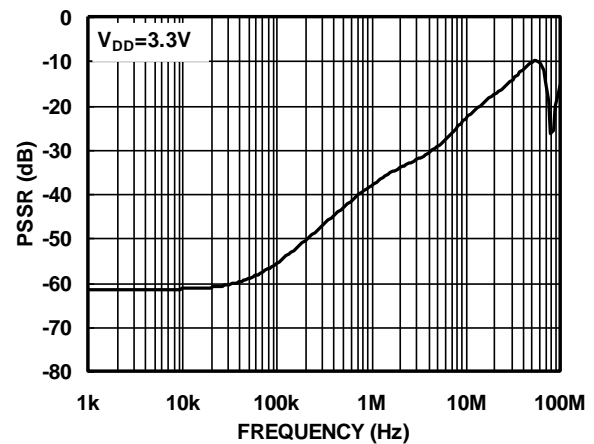


Figure 8 PSRR Vs. Frequency (FHD)

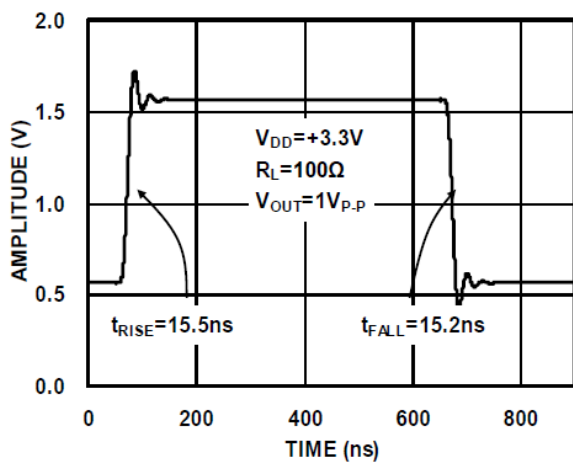


Figure 9 Large-Signal Pulse Response Vs. Time (HD Channel)

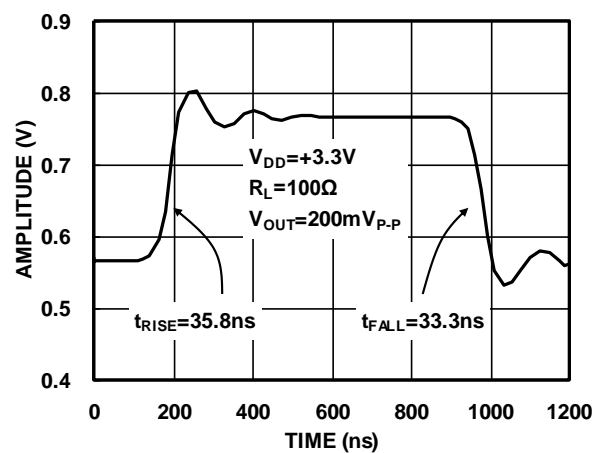


Figure 10 Small-Signal Pulse Response Vs. Time (SD Channel)

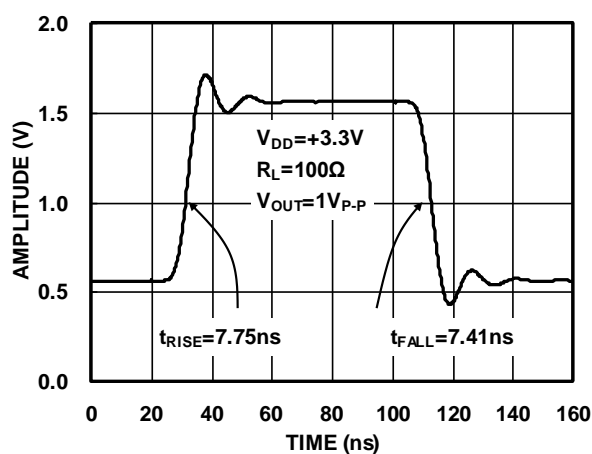


Figure 11 Large-Signal Pulse Response Vs. Time (FHD Channel)

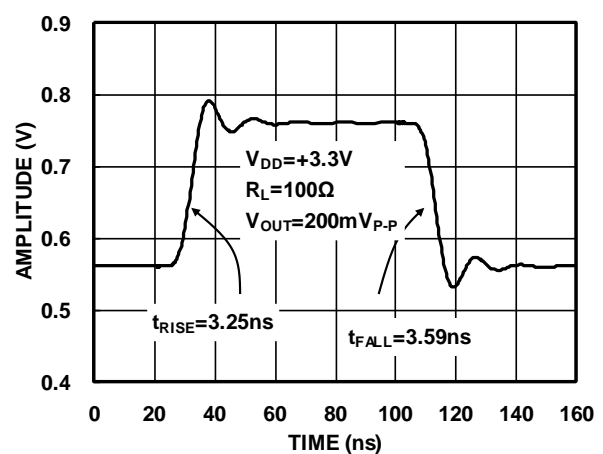


Figure 12 Small-Signal Pulse Response Vs. Time (FHD Channel)

## Detailed Description

### Functional Block Diagram

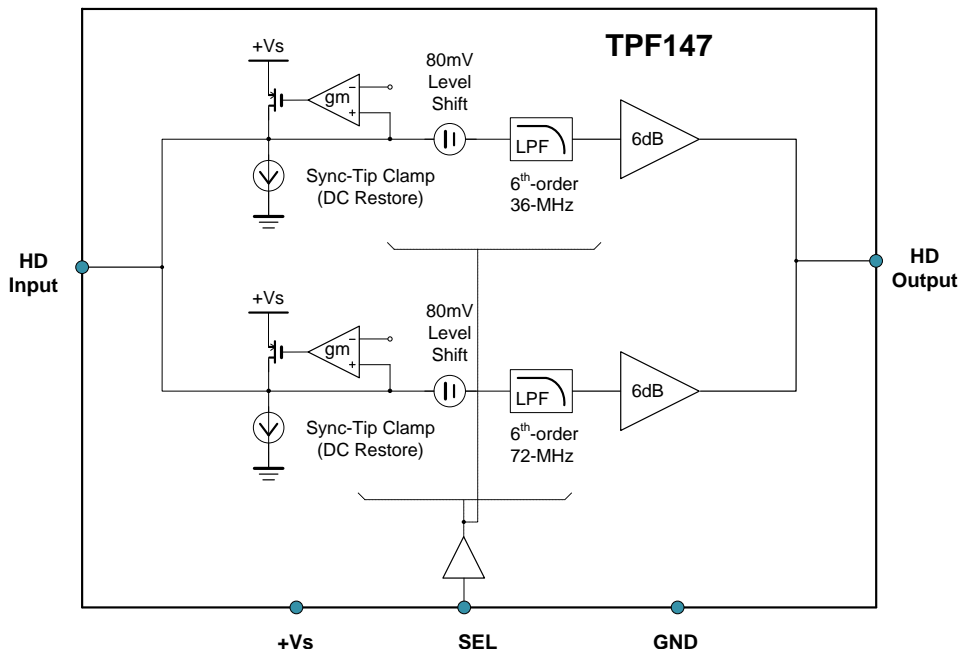


Figure 13 Functional Block Diagram

## Feature Description

### Internal Sync Clamp

The typical embedded video DAC operates from a ground-referenced single supply. This becomes an issue because the lower level of the sync pulse output may be at a 0 V reference level to some positive level. The problem is presenting a 0 V input to most single supply-driven amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degrading the video image. A larger positive reference may offset the input above its positive range.

The TPF147 features an internal sync clamp and offset function to level shift the entire video signal to the best level before it reaches the input of the amplifier stage. These features are also helpful to avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram of the TPF147 is shown in Figure 13. The AC-coupled video sync signal is pulled negative by a current source at the input of the comparator amplifier. When the sync tip goes below the comparator threshold the output comparator is driven negative, The PMOS device turns on clamping sync tip to near ground level. The network triggers on the sync tip of the video signal.

## Application and Implementation

### NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### Application Information

The TPF147 is targeted for systems that require a selectable full high-definition (FHD) video output for CVI video support and single high-definition (HD) video outputs. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the TPF147. The TPF147 incorporates many features not typically found in integrated video parts while the power consumption is very low.

### Typical Application

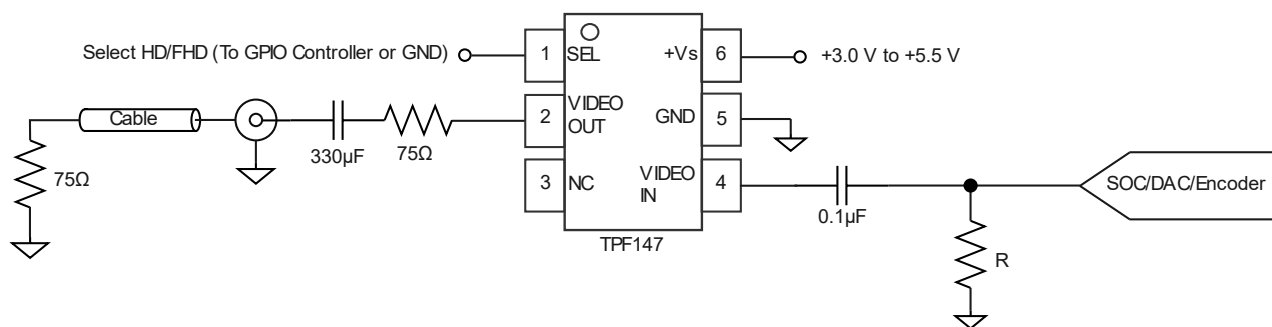


Figure 14 Typical AC-Coupled Application Circuit

### Droop Voltage and DC Restoration

The selection of the input AC-coupling capacitance is based on the system requirements. A typical sync tip width of a 64  $\mu$ s NTSC line is 4  $\mu$ s during which the clamp circuit restores its DC level. In the remaining 60  $\mu$ s period, the voltage droops because of a small constant 2.0  $\mu$ A sinking current. If the AC-coupling capacitance is 0.1  $\mu$ F, the maximum droop voltage is about 1 mV which is restored by the clamp circuit. The maximum pull-up current of the clamp circuit is 1.7 mA. For a 4  $\mu$ s sync tip width and a 0.1  $\mu$ F capacitor, the maximum restoration voltage is about 80 mV.

The line droop voltage will increase if a smaller AC-coupling capacitance is used. For the same reason, if a larger capacitance is used the line droop voltage will decrease.

### Low Pass Filter--Sallen Key

The Sallen Key is a classic low-pass configuration. This provides a very stable low-pass function, and in the case of the TPF147, two six-pole roll-offs are at around 36 MHz and 72 MHz. The six-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key.

### Output Couple

The TPF147 output could support both "AC Couple" and "DC Couple", if "AC Couple" is used, this capacitor's value is typically between 220- $\mu$ F and 1000- $\mu$ F, although 470- $\mu$ F is common. The value of this capacitor must

be so large that it can minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously.

The TPF147's internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, thereby saving board space and additional expense for capacitors. This makes the TPF147 extremely attractive for portable video applications. Additionally, this solution completely eliminates the issue of field tilt in the lower frequency. The trade-off is a greater demand of supply current. The typical load current for AC coupled is around 1 mA, compared to typical 6.6 mA used when DC coupling.

### Output Drive Capability and Power Dissipation

With the high output drive capability of the TPF147, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure the operation of the amplifier in a safe operating area. The maximum power dissipation allowed in a package is determined according to the Equation:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where:

$T_{JMAX}$  = Maximum junction temperature

$T_{AMAX}$  = Maximum ambient temperature

$\theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or for sourcing:

$$PD_{MAX} = V_s \times I_{SMAX} + (V_s - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

Where:

$V_s$  = Supply voltage

$I_{SMAX}$  = Maximum quiescent supply current

$V_{OUT}$  = Maximum output voltage of the application

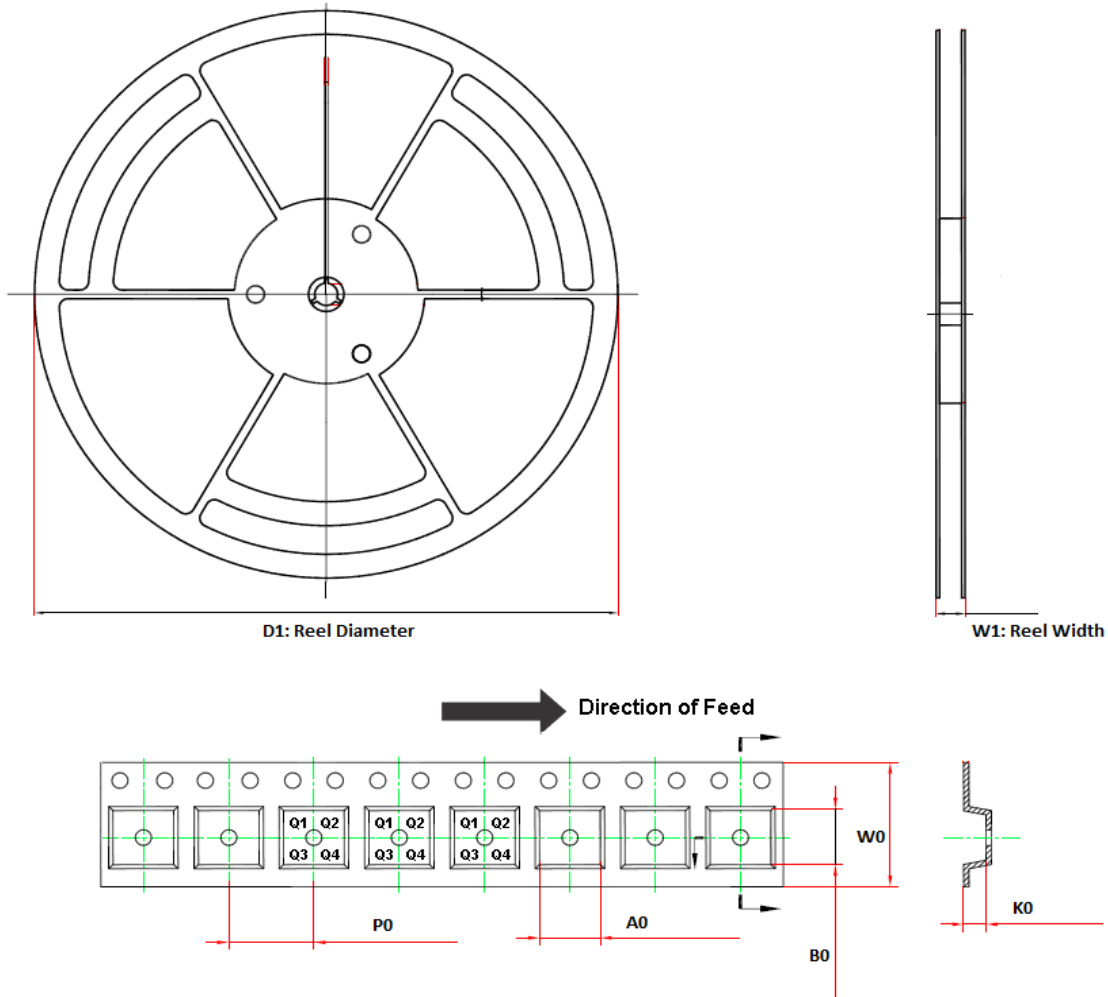
$R_{LOAD}$  = Load resistance tied to ground

By setting the two  $PD_{MAX}$  equations equal to each other, we can solve the output current and  $R_{LOAD}$  to avoid the device overheated.

### Power Supply Bypassing Printed Circuit Board Layout

As with any modern operational amplifier, a well-printed circuit board layout is necessary for an optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7  $\mu$ F tantalum capacitor in parallel with a 0.1  $\mu$ F ceramic capacitor from + $V_s$  to GND will suffice.

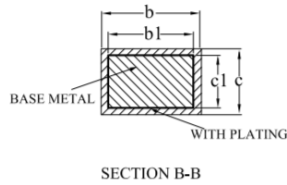
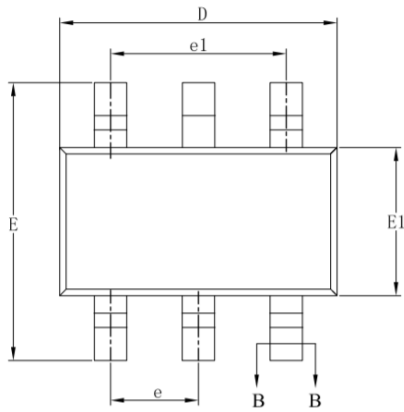
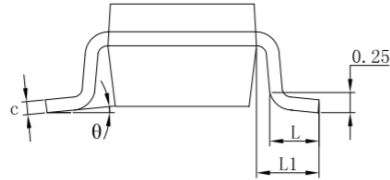
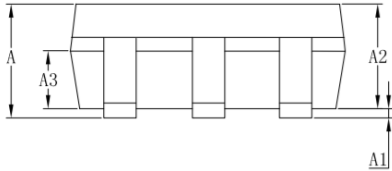
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPF147-TR	SOT23-6	178	12.3	3.2	3.2	1.4	4	8	Q3

### Package Outline Dimensions

#### SOT23-6



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	—	0.60
θ	0	—	8°

**Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPF147-TR	-40 to 85°C	SOT23-6	F47	3	Tape and Reel, 3000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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