
Quad Channel Jitter Cleaner Digital PLL

Features

- Quad DPLLs synchronize any physical layer clocks, provides arbitrary frequency translation with jitter cleaning
- Ultra-low jitter of 80fs rms
- Output frequency range:
 - Differential: 8kHz to 1500MHz
 - Single-ended: 1Hz to 250MHz
 - Format: LVDS/LVPECL/HCSL/CMOS with programmable signal amplitude
- Input frequency range
 - Differential: 8kHz to 1000MHz
 - Single-ended: 1Hz to 250MHz
 - Format: LVDS/LVPECL/HCSL/CMOS
- Programmable digital loop filter bandwidth: 1mHz to 4kHz
- Flexible MUXs routes any input to any output
- Automatic and manual holdover and reference switchover, providing zero delay, hitless or phase buildout operation
- Programmable priority-based reference switching with manual / automatic revertive / non-revertive modes supported
- Excellent phase buildout reference switching for 8kHz/ 19.44MHz/25MHz/38.88MHz to minimize output phase transient
- Fast lock feature for low loop bandwidths
- DCO mode: frequency resolution down to 1ppt (1e-12)
- Reference monitor (reliable and fast validation), programmable
- Delay adjustment on reference, feedback path and output channel
- Delay adjustment on output (coarse / fine delay)
- Phase Slope Limited Reference Switching (PSLRS)
- In-circuit programmable with non-volatile memory (NVM)
- Core voltage
 - VDD: 1.8V+/-5%;
 - VDDA: 3.3V+/-5%
- Independent output clock supply pins: 3.3V, 2.5V, or 1.8V +/-5%
- Serial interface: SPI or I2C
- Package: 64-QFN 9x9 mm

- Temperature range: -40C to +85C

- Pb-free, RoHS-6 compliant

- Complies with ITU-T G.8262 EEC-Option 1 and EEC-Option 2 and G.8262.1

Applications

- Router/Switch
- PTN/OTN/PON/xDSL
- Macro CellBBU/AAU
- Small Cell Radio

Description

The TPK1031 is a four-channel digital phase locked loop (DPLL) that supports arbitrary frequency conversion. The frequency range of the reference input is from 1Hz to 1000MHz, and the output frequency range can reach up to 1500MHz. The typical jitter output for 12kHz~20MHz is 80fs. It has four reference inputs and ten differential output channels. Excellent reference switching capability makes it well suited for handling reference switching in various conditions, either internal or external reference switching. The TPK1031 can be utilized in wireless base stations and wired communication systems.

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TPK1031

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Product Family Table

| Order Number | DPLLs | References | Outputs | Applications | Package |
|------------------|-------|------------|---------|------------------|-----------|
| TPK1031L1-VS1R | 4 | 4 | 10 | Wired / Wireless | QFN9x9-64 |
| TPK1031L1-VS1R-S | 4 | 4 | 10 | Wired / Wireless | QFN9x9-64 |

Revision History

| Date | Revision | Notes |
|----------|----------|-----------------|
| 2023-5-8 | Rev.A1 | Initial Version |

Typical Performance

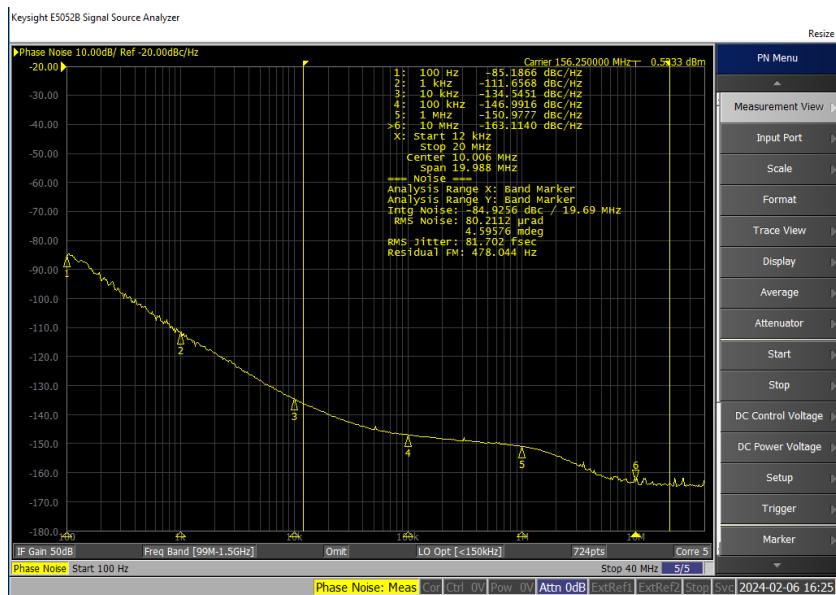


Figure 1. 156.25MHz Phase Noise

Test Setup: Output Clock = 156.25MHz, System clock = 54MHz XTAL

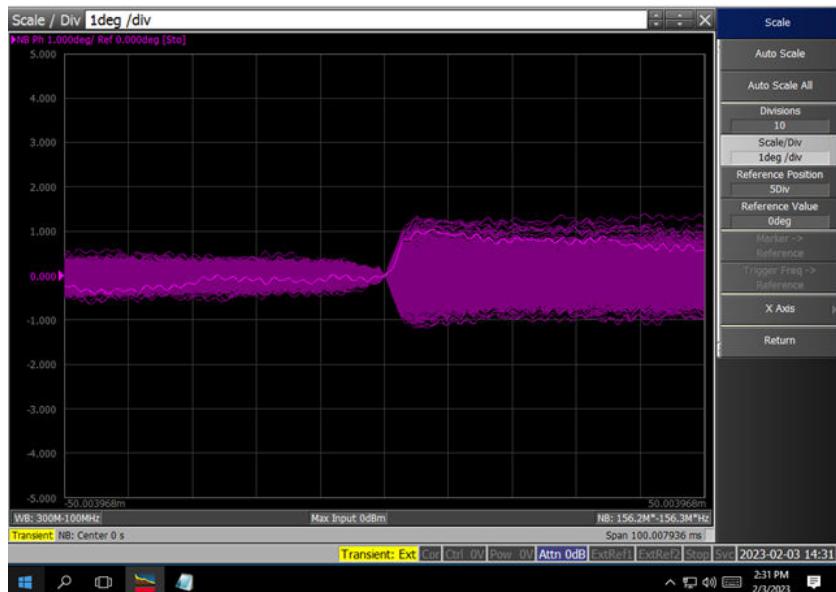
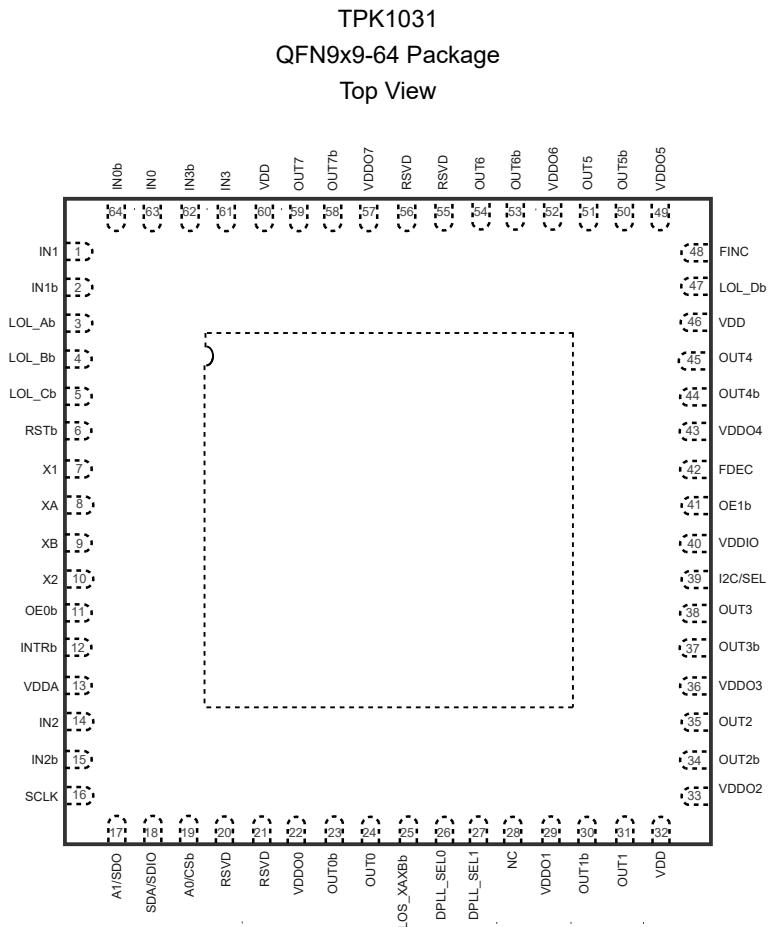


Figure 2. 156.25MHz Output Phase Transient

TPK1031 Output Phase Transient when reference switchover with iteration = 10000. Maximum phase shift <1.3ps @156.25MHz

Test Setup: System Clock=54MHz XTAL, REF0=200KHz DPFD (25MHz IN), REF1=200KHz DPFD (25MHz IN), OUT0=156.25MHz, DPLL lock to REF0 or REF1, Control DPLL to manual select REF0 or REF1DPLL0, Phase Build Out (PBO) Switch Enabled. Using E5052 to record the OUT0 output phase transientSwitch Iteration 10,000

Pin Configuration and Functions



| Mnemonic | PIN No. | Type | Description |
|---------------|---------|------|---|
| Inputs | | | |
| XA | 8 | I | Crystal Input. Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). |
| XB | 9 | I | |
| X1 | 7 | I | XTAL Shield. |
| X2 | 10 | I | Connect these pins directly to the XTAL ground pins.. |
| IN0 | 63 | I | |
| IN0b | 64 | I | |
| IN1 | 1 | I | Clock Inputs. |
| IN1b | 2 | I | Reference clock inputs for synchronizing DPLL. They can be both differential and single-ended clock signals. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded when accepting a single-ended clock. IN3/IN3b can also be used for external zero delay feedback. |
| IN2 | 14 | I | |
| IN2b | 15 | I | |
| IN3/FB_IN | 61 | I | |
| IN3b/FB_INb | 62 | I | |

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| Outputs | | | |
|------------------|----|-----|--|
| OUT0 | 24 | O | |
| OUT0b | 23 | O | |
| OUT1 | 31 | O | |
| OUT1b | 30 | O | |
| OUT2 | 35 | O | |
| OUT2b | 34 | O | |
| OUT3 | 38 | O | |
| OUT3b | 37 | O | |
| OUT4 | 45 | O | |
| OUT4b | 44 | O | |
| OUT5 | 51 | O | |
| OUT5b | 50 | O | |
| OUT6 | 54 | O | |
| OUT6b | 53 | O | |
| OUT7 | 59 | O | |
| OUT7b | 58 | O | |
| Serial Interface | | | |
| I2C_SEL | 39 | I | <p>I2C Select.</p> <p>Selects the serial interface mode as I2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). Internally pulled high.</p> |
| SDA/SDIO | 18 | I/O | <p>Serial Data Interface.</p> <p>Bidirectional data pin (SDA) for the I2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. An external resistor of at least 1kΩ is needed in I2C mode. In SPI mode, no external pull up resistor is required. Tie low when unused.</p> |
| A1/SDO | 17 | I/O | <p>Address Select 1/Serial Data Output.</p> <p>In I2C mode, it functions as the hardware controlled address A0. In 4-wire SPI mode this output is a push pull driver and functions as the serial data output (SDO) pin. Leave disconnected when unused.</p> |
| SCLK | 16 | I | <p>Serial Clock Input.</p> <p>This pin functions as the serial clock input for both I2C and SPI modes. When in I2C mode, this pin must be pulled-up using an external resistor of >1 kΩ. No pull-up resistor is needed when in SPI mode.</p> |
| A0/CSb | 19 | I | <p>Address Select 0/Chip Select.</p> <p>This pin functions as the hardware controlled address A0 in I2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up.</p> |
| Control/Status | | | |
| INTRb | 12 | O | <p>Interrupt.</p> <p>This pin is asserted low when a change in device status has occurred.</p> |

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| | | | |
|-----------|----|---|--|
| RSTb | 6 | I | Device Reset. Active low. Resets all internal logic to a known state and forces the device registers to their default values. This pin is internally pulledup. |
| OE0b | 11 | I | Output Enable 0. This pin is used to enable (low) and disable (high) the output clocks. By default this pin controls all outputs. It can also be configured to control a subset of outputs. This pin is internally pulled-down. |
| OE1b | 41 | I | Output Enable 1. This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. There is no internal pullup/pull-down for this pin. This pin must be pulled up or down externally (do not leave floating when not in use). |
| LOL_0b | 3 | O | Loss Of Lock_DPLL0/1/2/3. These output pins indicate when DPLL0, 1, 2, 3 is out-of-lock (low) or locked (high). |
| LOL_1b | 4 | O | |
| LOL_2b | 5 | O | |
| LOL_3b | 47 | O | |
| LOS_XAXBb | 25 | O | Loss of Signal on XA/XB Pin. A loss of signal alarm on the XA/XB pins. |
| DPLL_SEL0 | 26 | I | DPLL Select Pins. |
| DPLL_SEL1 | 27 | I | These pins are used in conjunction with the FINC and FDEC pins. The DPLL_SEL[1:0] pins determine which DPLL is affected by a frequency change using the FINC and FDEC pins. These pins are internally pulled-down. |
| FDEC | 42 | I | Frequency Decrement Pin. This pin is used to step-down the output frequency of a selected DPLL. The frequency change step size is register configurable. The DPLL that is affected by the frequency change is determined by the DPLL_SEL[1:0] pins. |
| FINC | 48 | I | Frequency Increment Pin. This pin is used to step-up the output frequency of a selected DPLL. The frequency change step size is register configurable. The DPLL that is affected by the frequency change is determined by the DPLL_SEL[1:0] pins. |
| RSVD | 20 | | Reserved. Leave disconnected. |
| | 21 | | |
| | 55 | | |
| | 56 | | |
| NC | 28 | | No Connect. |
| Power | | | |
| VDD | 32 | P | Core Supply Voltage. |
| | 46 | P | The device core operates from a 1.8 V supply. A 0402 1µF capacitor should be placed very near each of these pins. |
| | 60 | P | |
| VDDA | 13 | P | Core Supply Voltage 3.3 V. This core supply pin requires a 3.3V power source. A 0402 1 µF capacitor should be placed very near each of these pins. |

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| | | | |
|---------|----|---|---|
| VDDIO | 40 | P | Digital IO Voltage. Connect to either 3.3 V or 1.8 V. A 0.1 μ F bypass capacitor should be placed very close to this pin. |
| VDDO0 | 22 | P | |
| VDDO1 | 29 | P | |
| VDDO2 | 33 | P | |
| VDDO3 | 36 | P | Output Clock Supply Voltage 0-7. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTnb outputs. A 0.1 uF bypass capacitor should be placed close to this pin. |
| VDDO4 | 43 | P | |
| VDDO5 | 49 | P | |
| VDDO6 | 52 | P | |
| VDDO7 | 57 | P | |
| GND PAD | 65 | P | Ground Pad. This pad must be connected to ground for proper operation. |

Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | MIN | MAX | UNIT |
|---|-------------------|--|------------------|-------|--------|
| DC Supply Voltage | V _{DD} | | -0.5 | 3.8 | V |
| | V _{DDA} | | -0.5 | 3.8 | V |
| | V _{DDO} | | -0.5 | 3.8 | V |
| Input Voltage Range | V _{I1} | IN0~IN3 | -1 | 2.5 | V |
| | V _{I2} | RSTb, OE0b, OE1b, I2C_SEL, FINC, FDEC, DPLL_SEL[1:0], SDA/SDIO, A1/SDO, SCLK, A0/CSb | -0.5 | 3.8 | V |
| | V _{I3} | XA/XB | -0.5 | 2.7 | V |
| Latch-up Tolerance | LU | | JESD78 Compliant | | |
| ESD Tolerance | HBM | 100pF, 1.5kohm | | 2 | kV |
| Max junction temperature | T _J | | | | 125° C |
| Storage temperature | T _{stg} | | -55 | 150 | °C |
| Soldering temperature | T _{peak} | | | 260 | °C |
| Soldering temperature time at T _{peak} | T _p | | | 20-40 | s |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD(Electrostatic Discharge Protection)

| Parameter | Symbol | Test Conditions | VALUE | UNIT |
|----------------------|--------|------------------------------|-------|------|
| ESD-Human Body Model | HBM | 100pF, 1.5kohm, all pins (1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

| Parameter | Symbol | MIN | NOM | MAX | UNIT | |
|---|------------|------|------|------|------|--|
| Ambient Temperature | T_A | -40 | 25 | 85 | °C | |
| Board Temperature | T_B | | | 105 | °C | |
| Junction Temperature | T_{JMAX} | | | 125 | °C | |
| Core Supply Voltage | V_{DD} | 1.71 | 1.80 | 1.89 | V | |
| | V_{DDA} | 3.14 | 3.30 | 3.47 | V | |
| Output Driver Supply Voltage | V_{DDO} | 3.14 | 3.30 | 3.47 | V | |
| | | 2.38 | 2.50 | 2.63 | | |
| | | 1.71 | 1.80 | 1.89 | | |
| Status Pin Supply Voltage | V_{DDS} | 3.14 | 3.30 | 3.47 | V | |
| | | 1.71 | 1.80 | 1.89 | | |
| Note: | | | | | | |
| 1. Min/Max specification are design guaranteed. | | | | | | |
| 2. Typical values apply at nominal supply voltage and operating temperature of 25°C | | | | | | |

Thermal Information

| Parameter | Symbol | 64-QFN | UNIT | Condition |
|--|---------------------------|--------|------|---------------|
| Junction-to-ambient thermal resistance | Θ_{JA} | 22.2 | °C/W | Still air |
| | | 19.4 | °C/W | Air Flow 1m/s |
| | | 18.3 | °C/W | Air Flow 2m/s |
| Junction-to-case (top) thermal resistance | $\Theta_{JC}(\text{top})$ | 9.5 | °C/W | |
| Junction-to-board thermal resistance | Θ_{JB} | 9.4 | °C/W | |
| Junction-to-board characterization parameter | Ψ_{JB} | 9.3 | °C/W | |
| Junction-to-top characterization parameter | Ψ_{JT} | 0.2 | °C/W | |
| Note: | | | | |
| 1. 64-QFN: Based on PCB Dimension: 3" x 4.5" PCB Thickness: 1.6mm, PCB Land/Via: 36, Number of Cu Layers: 4. | | | | |

Electrical Characteristics

All minimum/maximum specifications at $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ and all typical specifications at $T_J = 25^\circ\text{C}$

$T_J = -40^\circ\text{C}$ to 125°C , ($\text{DVDD} = 1.8 \text{ V} \pm 5\%$, $\text{AVDD} = 3.3 \text{ V} \pm 5\%$, $\text{VDDIO} = 3.3 \text{ V} \pm 5\%$, $1.8 \text{ V} \pm 5\%$, $\text{VDDO} = 1.8 \text{ V} \pm 5\%$, $2.5 \text{ V} \pm 5\%$, or $3.3 \text{ V} \pm 5\%$)

Table 1. DC Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------------|-----------|---------------------|-----|------|-----|------|
| Core Supply Current | I_{DD} | TPK1031, 4 DPLLs | — | 320 | - | mA |
| | | TPK1031,, 1 DPLL | — | 200 | - | mA |
| | I_{DDA} | TPK1031,, 4 DPLLs | — | 155 | - | mA |
| | | TPK1031,, 1 DPLL | — | 125 | - | mA |
| Output Buffer Supply Current | I_{DDO} | 2.5 V LVPECL Output | — | 22 | - | mA |
| | | 2.5 V LVDS Output | — | 15 | - | mA |
| | | 3.3 V LVCMS Output | — | 22 | - | mA |
| | | 2.5 V LVCMS Output | — | 18 | - | mA |
| | | 1.8 V LVCMS Output | — | 12 | - | mA |
| Total Power Dissipation | P_d | TPK1031,, 4 DPLLs | — | 1400 | - | mW |
| | | TPK1031,, 2 DPLLs | — | 1100 | - | mW |

Notes:

1. TPK1031, configuration: 7x2.5V LVDS outputs @ 156.25MHz. No power in termination resistors
2. Differential output termination: 100ohm load with ac coupled.
3. CMOS driver setup: 3

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VDD = 3.3 V \pm 5%, VDDO = 1.8 V \pm 5%, 2.5 V \pm 5%, or 3.3 V \pm 5%, TA = –40 to 85 °C

Table 2. DPLL Performance Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------|--|-----|-----|-------|---------|
| PLL Loop Bandwidth Programming Range | f_{BW} | | 0.1 | — | 4000 | Hz |
| Initial Start-Up Time | t_{START} | Time from power-up to when the device generates free-running clocks | 89 | - | 126 | ms |
| PLL Lock Time | t_{ACQ} | With fastlock enabled, $f_{IN}=19.44$ MHz, dpll loop bandwidth=50Hz | — | 1.7 | | ms |
| POR to Serial Interface Ready | t_{RDY} | | — | — | | ms |
| Maximum Phase Transient During a Hitless Switch | t_{SWITCH} | Single automatic/manual switch between two 8 kHz inputs, DPLL BW = 40 Hz | — | — | 150 | ps |
| | | Single automatic/manual switch between two 2MHz inputs, DPLL BW = 400 Hz | — | — | 80 | ps |
| Input-to-Output Delay Variation | $t_{IODELAY}$ | $f_{IN}=f_{OUT}=2$ MHz DPLL BW=4kHz | — | — | 0.02 | ns |
| | | $f_{IN}=f_{OUT}=62$ kHz DPLL BW=4 kHz | — | — | 0.05 | ns |
| | | $f_{IN}=f_{OUT}=8$ kHz DPLL BW=4 kHz | — | — | 0.3 | ns |
| Jitter Peaking | J_{PK} | Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a loop bandwidth of 4 Hz | — | — | 0.1 | dB |
| Jitter Tolerance | J_{TOL} | Compliant with G.8262 Options 1 and 2 for 1G, 10G or 25G Synchronous Ethernet Jitter Modulation Frequency=10Hz | — | | 31.25 | UIpk-pk |
| Pull-in Range | ω_P | | — | 500 | 20000 | ppm |
| RMS Phase Jitter | J_{GEN} | 12 kHz to 20 MHz | — | 85 | 110 | fs |

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VDD = 1.8 V \pm 5%, VDDA = 3.3 V \pm 5%, TA = -40 to 85 °C

Table 3. DPLL Input Clock and System Clock Reference Input Spec

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|--|----------|-----|------|------------|
| Standard Differential or Single-Ended - AC Coupled Input Buffer (IN0/IN0b, IN1/IN1b, IN2/IN2b, IN3/IN3b) | | | | | | |
| Input Frequency Range | f_{IN} | Differential | 0.008 | — | 1500 | MHz |
| | | All Single-ended signals (including LVC MOS) | 0.000001 | — | 250 | MHz |
| Voltage Swing | V_{IN} | Differential ac-coupled $f_{IN} < 250$ MHz | 100 | — | 1800 | mVpp_se |
| | | Differential ac-coupled 250 MHz $< f_{IN} < 750$ MHz | 225 | — | 1800 | mVpp_se |
| | | Single-ended ac-coupled $f_{IN} < 250$ MHz | 100 | — | 3600 | mVpp_se |
| Slew Rate | SR | | 400 | — | — | V/ μ s |
| Duty Cycle | DC | | 40 | — | 60 | % |
| Input Capacitance | C_{IN} | | — | 2.4 | — | pF |
| Input Resistance Differential | R_{IN_DIFF} | | — | 16 | — | k Ω |
| Input Resistance Single-ended | R_{IN_SE} | | — | 8 | — | k Ω |
| LVC MOS / Pulsed CMOS DC-Coupled Input Buffer (IN0, IN1, IN2, IN3) | | | | | | |
| Input Frequency | f_{IN_CMOS} | Standard CMOS & Non-standard CMOS | 0.000001 | — | 250 | MHz |
| | | Pulsed CMOS | 0.000001 | — | 1 | MHz |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------------|--|-------|-----|-------|------------|
| Input Voltage | V_{IL} | Standard CMOS | — | — | 0.5 | V |
| | | Non-standard CMOS & Pulsed CMOS | — | — | 0.4 | V |
| | V_{IH} | Standard CMOS | 1.3 | — | — | V |
| | | Non-standard CMOS & Pulsed CMOS | 0.8 | — | — | V |
| Slew Rate | SR | | 400 | — | — | V/ μ s |
| Duty Cycle | DC | Standard CMOS & Non-standard CMOS | 40 | — | 60 | % |
| | | Pulsed CMOS | 5 | | 95 | |
| Minimum Pulse Width | PW | Standard CMOS & Non-standard CMOS (250 MHz @ 40% Duty Cycle) | 1.6 | — | — | ns |
| | | Pulsed CMOS (1 MHz @ 40% Duty Cycle) | 50 | — | — | |
| Input Resistance | R_{IN} | | — | 8 | — | k Ω |
| | | | | | | |
| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
| REFCLK (Applied to XA/XB) | | | | | | |
| REFCLK Frequency | f_{IN_REF} | Full operating range. Jitter performance may be reduced. | 24.97 | — | 54.06 | MHz |
| | | Range for best jitter. | 48 | — | 54 | MHz |
| Input Voltage Swing | V_{IN_DIFF} | | 365 | — | 2500 | mVpp_diff |
| | V_{IN_SE} | | 365 | — | 2000 | mVpp_se |
| Slew rate | SR | | 400 | — | — | V/ μ s |
| Input Duty Cycle | DC | | 40 | — | 60 | % |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--|----------------|-----|-----|-----|------|
| Notes: | | | | | | |
| 1. | Voltage swing is specified as single-ended signal. Unit: mVpp | | | | | |
| 2. | Rise time and fall time using equation: tr/tf80-20 = ((0.8 - 0.2) x VIN_Vpp_se) / SR | | | | | |

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VDD = 3.3V \pm 5%, VDDO = 1.8 V \pm 5%, 2.5 V \pm 5%, or 3.3 V \pm 5%, TA = -40 to 85 °C

Table 4. Differential Clock Output Specifications

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|--|---------------|--|--------------|------------|------------|------------|-------------|
| Output Frequency | f_{OUT} | | | 0.008 | — | 1500 | MHz |
| Duty Cycle | DC | $f_{OUT} < 400$ MHz | | 48 | — | 52 | % |
| | | 400 MHz $< f_{OUT} < 1500$ MHz | | 45 | — | 55 | % |
| Output Voltage Amplitude | V_{OUT} | $V_{DDO} = 3.3$ V, 2.5 V, or 1.8 V | LVDS | 350 | 450 | 530 | mVpp_se |
| | | $V_{DDO} = 3.3$ V, 2.5 V | LVPECL | 630 | 750 | 950 | mVpp_se |
| Common Mode Voltage | V_{CM} | $V_{DDO} = 3.3$ V | LVDS | 1.1 | 1.2 | 1.3 | V |
| | | | LVPECL | 1.9 | 2 | 2.1 | V |
| | | $V_{DDO} = 2.5$ V | LVPECL, LVDS | 1.1 | 1.2 | 1.3 | V |
| | | $V_{DDO} = 1.8$ V | sub-LVDS | 0.8 | 0.9 | 1 | V |
| Output-to-Output Skew (Same DPLL, Different Outputs) | T_{SKS} | $f_{OUT} = 720$ MHz (LVDS differential) | | — | 0 | 75 | ps |
| OUT-OUTb Skew (Same Output) | T_{SK_OUT} | Measured from positive to negative output pins | | — | 0 | 50 | ps |
| Rise and Fall Times | t_r / t_f | $f_{OUT} > 100$ MHz (20% to 80%) | | — | 100 | 200 | ps |
| Differential Output Impedance | Z_o | | | — | 100 | — | Ω |
| Power Supply Noise Rejection | PSRR | 10 kHz sinusoidal noise | | — | -101 | — | dBc |
| | | 100 kHz sinusoidal noise | | — | -96 | — | dBc |
| | | 500 kHz sinusoidal noise | | — | -99 | — | dBc |
| | | 1 MHz sinusoidal noise | | — | -97 | — | dBc |
| Output-output Crosstalk | XTALK | | | — | -72 | — | dB |

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VDD = 3.3 V \pm 5%, VDDO = 1.8 V \pm 5%, 2.5 V \pm 5%, or 3.3 V \pm 5%, TA = –40 to 85 °C)

Table 5. LVC MOS Clock Output Specifications

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------|------------------|--------------------------------------|--------------------------|-----|-----|------|
| Output Frequency | f _{OUT} | | 0.000001 | — | 250 | MHz |
| Duty Cycle | DC | f _{OUT} < 100 MHz | 48 | — | 52 | % |
| | | 100 MHz < f _{OUT} < 250 MHz | 44 | — | 56 | |
| Output Voltage High | V _{OH} | V _{DDO} = 3.3 V | | | | |
| | | OUTx_CMOS_DRV=1 | I _{OH} = –10 mA | — | — | V |
| | | OUTx_CMOS_DRV=2 | I _{OH} = –12 mA | — | — | |
| | | OUTx_CMOS_DRV=3 | I _{OH} = –17 mA | — | — | |
| | | V _{DDO} = 2.5 V | | | | |
| | | OUTx_CMOS_DRV=1 | I _{OH} = –6 mA | — | — | V |
| | | OUTx_CMOS_DRV=2 | I _{OH} = –8 mA | — | — | |
| | | OUTx_CMOS_DRV=3 | I _{OH} = –11 mA | — | — | |
| | | V _{DDO} = 1.8 V | | | | |
| | | OUTx_CMOS_DRV=2 | I _{OH} = –4 mA | — | — | V |
| | | OUTx_CMOS_DRV=3 | I _{OH} = –5 mA | — | — | |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit | |
|---------------------|---------------------------------|--------------------------|--------------------------|-----|-----|-------------------------|----|
| Output Voltage Low | V _{OL} | V _{DDO} = 3.3 V | | | | | |
| | | OUTx_CMOS_DRV=1 | I _{OL} = 10 mA | — | — | V _{DDO} x 0.15 | |
| | | OUTx_CMOS_DRV=2 | I _{OL} = 12 mA | — | — | | |
| | | OUTx_CMOS_DRV=3 | I _{OL} = 17 mA | — | — | | |
| | | V _{DDO} = 2.5 V | | | | | |
| | | OUTx_CMOS_DRV=1 | I _{OL} = 6 mA | — | — | V _{DDO} x 0.15 | |
| | | OUTx_CMOS_DRV=2 | I _{OL} = 8 mA | — | — | | |
| | | OUTx_CMOS_DRV=3 | I _{OL} = 11 mA | — | — | | |
| | | V _{DDO} = 1.8 V | | | | | |
| | | OUTx_CMOS_DRV=2 | I _{OL} = 4 mA | — | — | V _{DDO} x 0.15 | |
| | | OUTx_CMOS_DRV=3 | I _{OL} = 5 mA | — | — | V _{DDO} x 0.15 | |
| Rise and Fall Times | t _r / t _f | (20% to 80%) | V _{DDO} = 3.3V | — | 400 | 600 | ps |
| | | | V _{DDO} = 2.5 V | — | 450 | 600 | ps |
| | | | V _{DDO} = 1.8 V | — | 550 | 750 | ps |

Quad Channel Jitter Cleaner Digital PLL

VDD=1.8V ±5%, VDDA=3.3V ±5%, VDDIO = 3.3V ±5%, 1.8V ±5%, TA = -40 to 85 °C

Table 6. Serial and Control Input Pin Specifications

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|----------------|-------------------------|-----|-------------------------|------|
| Serial and Control Input Pins (I2C_SEL, RSTb, OE0b, A1/SDO, SCLK, A0/CSb, FINC, A0/CSb, SDA/SDIO, DPLL_SEL[1:0]) | | | | | | |
| Input Voltage | V _{IL} | | — | — | 0.3 x V _{DDIO} | V |
| | V _{IH} | | 0.7 x V _{DDIO} | — | — | V |
| Input Capacitance | C _{IN} | | — | 2 | — | pF |
| Input Resistance | R _L | | — | 20 | — | kΩ |
| Minimum Pulse Width | PW | RSTb, FINC | 100 | — | — | ns |
| Update Rate | F _{UR} | FINC | — | — | 1 | MHz |
| Control Input Pins (FDEC, OE1b) | | | | | | |
| Input Voltage | V _{IL} | | — | — | 0.3 x V _{DDIO} | V |
| | V _{IH} | | 0.7 x V _{DDIO} | — | — | V |
| Input Capacitance | C _{IN} | | — | 2 | — | pF |
| Minimum Pulse Width | PW | FDEC | 100 | — | — | ns |
| Update Rate | F _{UR} | FDEC | — | — | 1 | MHz |

VDD = 1.8 V ±5%, VDDA = 3.3 V ±5%, VDDIO = 3.3 V ±5%, 1.8 V ±5%, TA=-40 to 85°C

Table 7. Output Serial and Status Pin Specifications

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|-------------------------|--------------------------|-----|-------------------------|------|
| Serial and Status Output Pins (LOL_Ab, LOL_Bb, LOL_Cb, LOL_Db, INTRb, LOS_XAXBb, SDA/SDIO, A1/SDO) | | | | | | |
| Output Voltage | V _{OH} | I _{OH} = -2 mA | 0.85 x V _{DDIO} | — | — | V |
| | V _{OL} | I _{OL} = 2 mA | — | — | 0.15x V _{DDIO} | V |

AC Timing Requirements

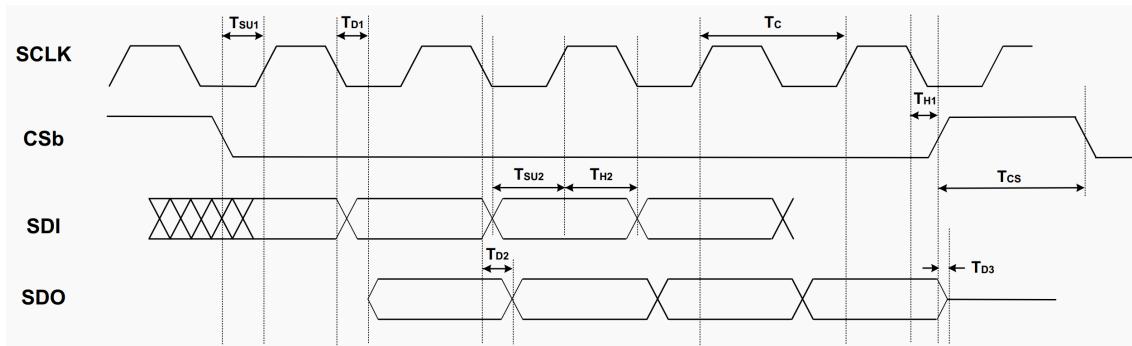
VDD=1.8V+/-5% , VDDA=3.3V+/-5%, VDDIO=3.3V+/-5%, 1.8V+/-5%, TA=-40°C to +85°C

Table 8. SPI Timing Specifications (4-Wires)

| Parameter | Symbol | MIN | Typ | MAX | UNIT |
|----------------|------------------|-----|-----|-----|------|
| SCLK Frequency | f _{SPI} | | | 20 | MHz |

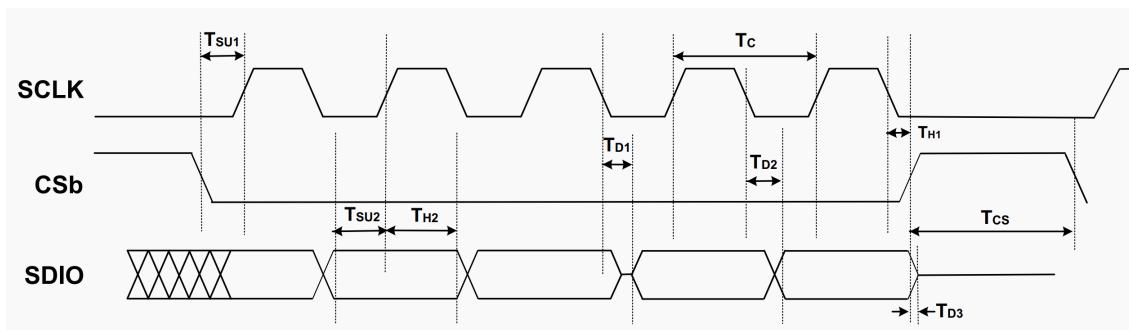
Quad Channel Jitter Cleaner Digital PLL

| Parameter | Symbol | MIN | Typ | MAX | UNIT |
|---------------------------------------|-----------|-----|-----|-----|------|
| SCLK Duty Cycle | T_{DC} | 40 | | 60 | % |
| SCLK Period | T_C | 50 | | | ns |
| Delay Time, SCLK Fall to SDO Active | T_{D1} | | | 18 | ns |
| Delay Time, SCLK Fall to SDO | T_{D2} | | | 15 | ns |
| Delay Time, CSb Rise to SDO Tri-State | T_{D3} | | | 15 | ns |
| Setup Time, CSb to SCLK | T_{SU1} | 5 | | | ns |
| Hold Time, SCLK Fall to CSb | T_{H1} | 5 | | | ns |
| Setup Time, SDI to SCLK Rise | T_{SU2} | 5 | | | ns |
| Hold Time, SDI to SCLK Rise | T_{H2} | 5 | | | ns |
| Delay Time Between Chip Select (CSb) | T_{CS} | 95 | | | ns |


Figure 3. 4-Wires SPI Timing

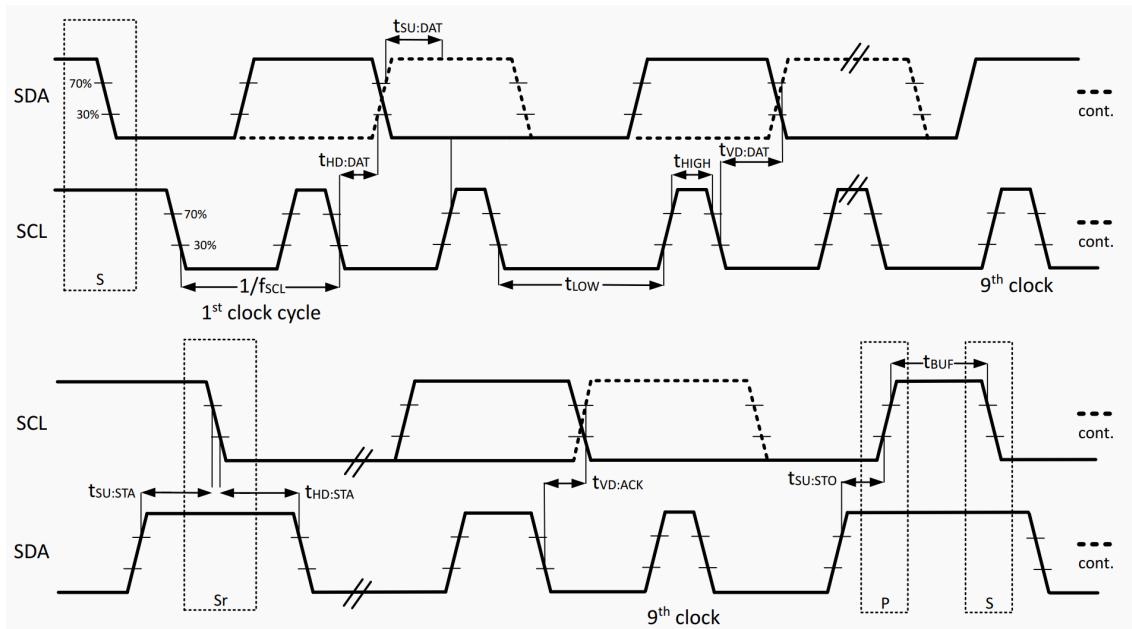
Quad Channel Jitter Cleaner Digital PLL
Table 9. I2C Timing Specifications (3-Wires)

| Parameter | Symbol | MIN | Typ | MAX | UNIT |
|---------------------------------------|-----------|-----|------|-----|------|
| SCLK Frequency | f_{SPI} | | | 20 | MHz |
| SCLK Duty Cycle | T_{DC} | 40 | | 60 | % |
| SCLK Period | T_c | 50 | | | ns |
| Delay Time, SCLK Fall to SDO Active | T_{D1} | | 12.5 | 18 | ns |
| Delay Time, SCLK Fall to SDO | T_{D2} | | 10 | 15 | ns |
| Delay Time, CSb Rise to SDO Tri-State | T_{D3} | | 10 | 15 | ns |
| Setup Time, CSb to SCLK | T_{SU1} | 5 | | | ns |
| Hold Time, SCLK Fall to CSb | T_{H1} | 5 | | | ns |
| Setup Time, SDI to SCLK Rise | T_{SU2} | 5 | | | ns |
| Hold Time, SDI to SCLK Rise | T_{H2} | 5 | | | ns |
| Delay Time Between Chip Select (CSb) | T_{cs} | 95 | | | ns |


Figure 4. 3-Wires SPI Timing

Quad Channel Jitter Cleaner Digital PLL
Table 10. I2C Timing Specifications

| Parameter | Symbol | Standard Mode 100kbps | | Fast Mode 400kbps | | UNIT |
|--|--------------|--------------------------|--------|----------------------|---------|---------|
| | | MIN | MAX | MIN | MAX | |
| SCL Clock Frequency | f_{SCL} | | | 100 | | 400 MHz |
| SMBus Timeout | | 2.5 | 35.0 | 25.0 | 35.0 ms | |
| Hold Time (Repeated) START condition | $t_{HD:STA}$ | 4.0 | | 0.6 | | us |
| Low Period of SCL Clock | t_{LOW} | 4.7 | | 1.3 | | us |
| High Period of SCL Clock | t_{HIGH} | 4.0 | | 0.6 | | us |
| Setup Time for a Repeated START condition | $t_{SU:STA}$ | 4.7 | | 0.6 | | us |
| Data Hold Time | $t_{HD:DAT}$ | 100.0 | | 100.0 | | ns |
| Data Setup Time | $t_{SU:DAT}$ | 250.0 | | 100.0 | | ns |
| Rise Time of both SDA and SCL Signals | t_r | | 1000.0 | 20.0 | 300.0 | ns |
| Fall Time of both SDA and SCL Signals | t_f | | 300.0 | | 300.0 | ns |
| Setup Time for STOP condition | $t_{SU:STO}$ | 4.0 | 4.0 | 0.6 | | us |
| Bus Free Time between a STOP and START Condition | t_{BUF} | 4.7 | 4.7 | 1.3 | | us |
| Data Valid Time | $t_{VD:DAT}$ | | | | 0.9 | us |
| Data Valid Acknowledge Time | $t_{VD:ACK}$ | | | | 0.9 | us |


Figure 5. I2C Timing (Stand Mode and Fast Mode)

(1) The test data is based on bench test and design simulation.

Detailed Description

Functional Block Diagram

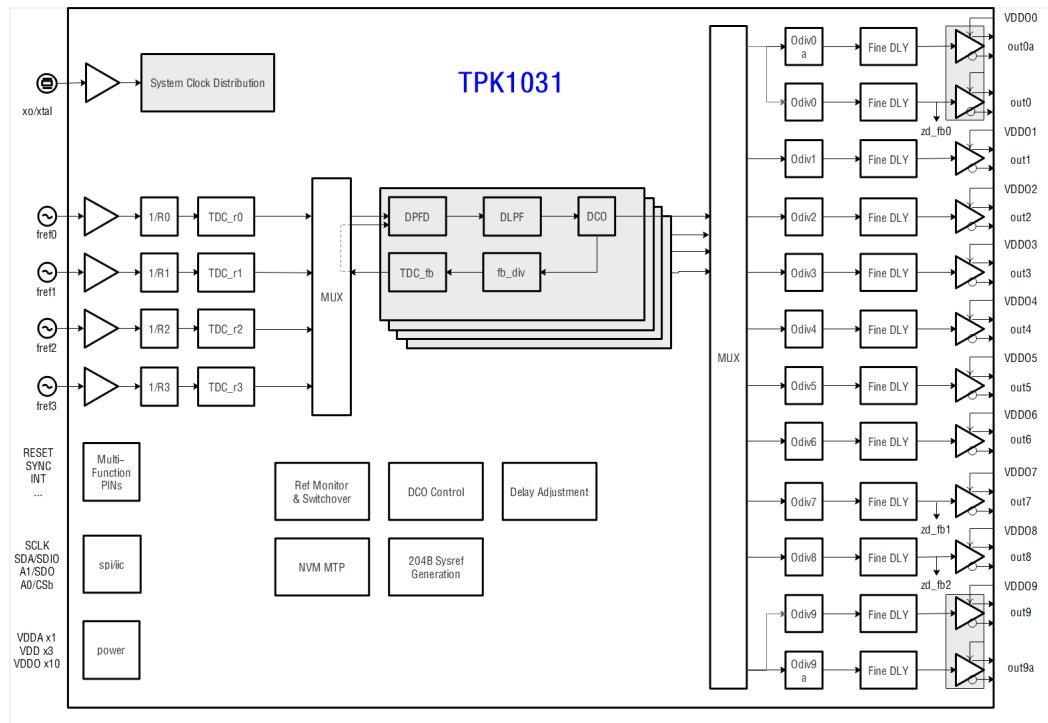


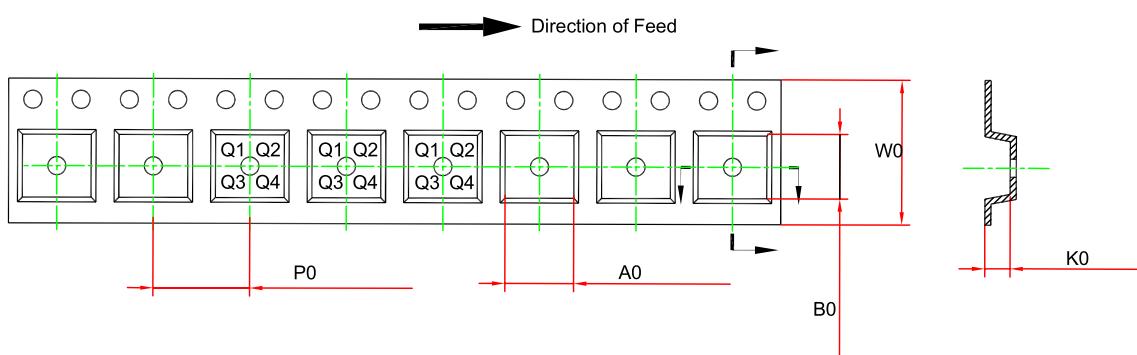
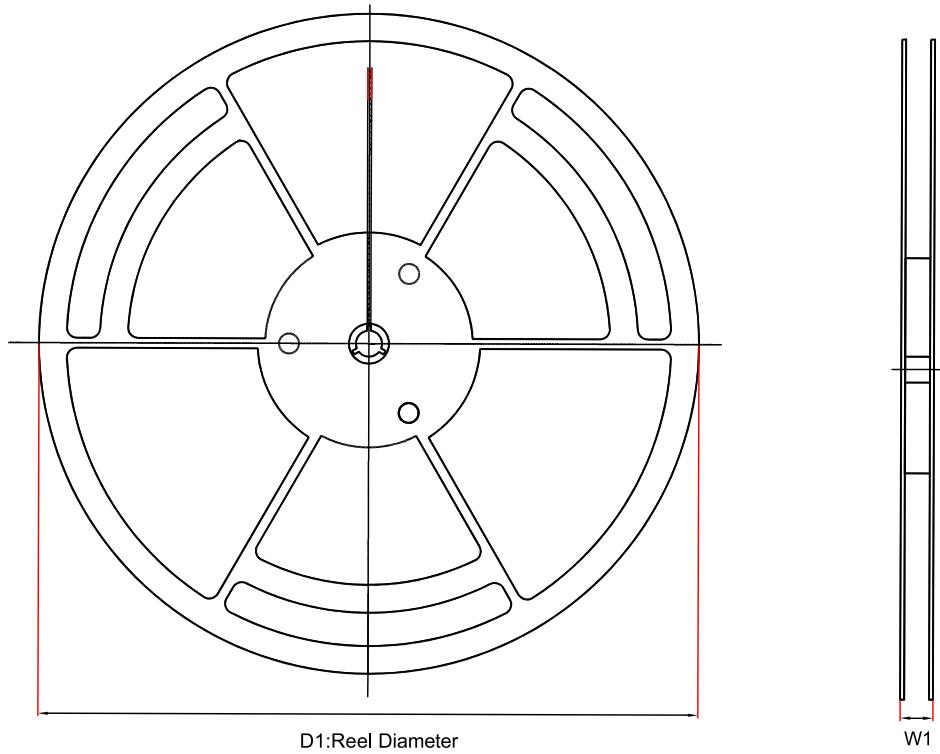
Figure 6. Functional Block Diagram

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Tape and Reel Information

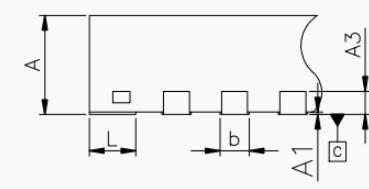
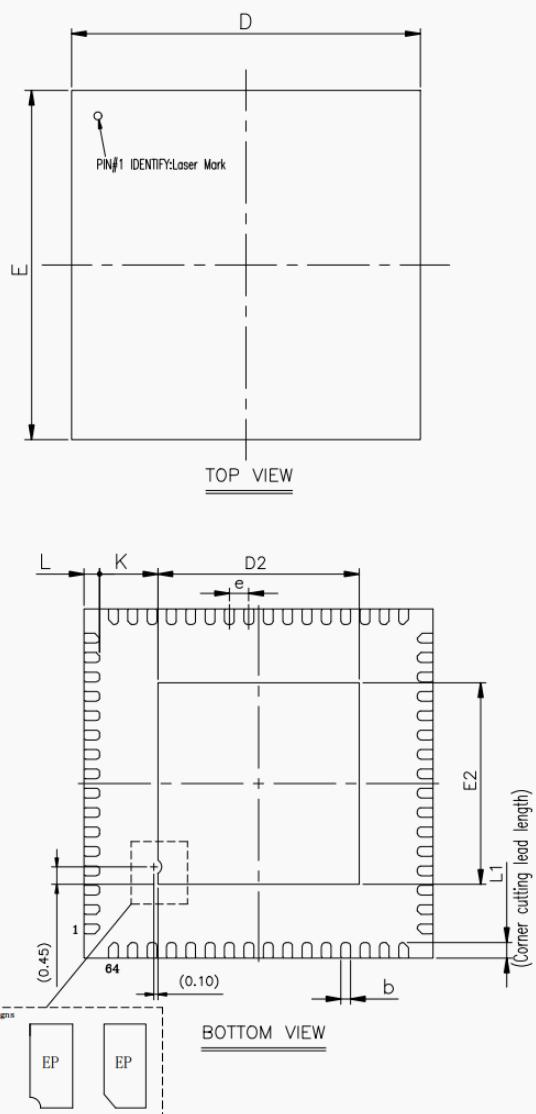


| Order Number | Package | D1 (mm) | W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | W0 (mm) | Pin1 Quadrant |
|------------------|-----------|---------|---------|---------|---------|---------|---------|---------|---------------|
| TPK1031L1-VS1R | QFN9x9-64 | 330 | 22.4 | 9.4 | 9.4 | 1.2 | 12 | 16 | Q1 |
| TPK1031L1-VS1R-S | QFN9x9-64 | 330 | 22.4 | 9.4 | 9.4 | 1.2 | 12 | 16 | Q1 |

Package Outline Dimensions

QFN9x9-64

Package Outline Dimensions QFT(QFN9X9-64-A)



DETAIL : "A"

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.800 | 0.900 | 0.031 | 0.035 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| A3 | 0.200 REF | | 0.008 REF | |
| D | 8.900 | 9.100 | 0.350 | 0.358 |
| E | 8.900 | 9.100 | 0.350 | 0.358 |
| e | 0.500 BSC | | 0.020 BSC | |
| D2 | 5.100 | 5.300 | 0.201 | 0.209 |
| E2 | 5.100 | 5.300 | 0.201 | 0.209 |
| K | 0.200 | | 0.008 | |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| L1 | 0.300 | 0.500 | 0.012 | 0.020 |

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Quad Channel Jitter Cleaner Digital PLL

Order Information

| Order Number | Operating Temperature Range | Package | Marking Information | MSL | Transport Media, Quantity | Eco Plan |
|------------------|-----------------------------|-----------|---------------------|------|---------------------------|----------|
| TPK1031L1-VS1R | -40 to 85°C | QFN9x9-64 | K1031 | MSL3 | Tape and Reel, 3000 | Green |
| TPK1031L1-VS1R-S | -40 to 85°C | QFN9x9-64 | S1031 | MSL3 | Tape and Reel, 3000 | Green |

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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TPK1031

Quad Channel Jitter Cleaner Digital PLL

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