3-A Output, High-PSRR, Low-Noise LDO Regulator

Features

- Input Voltage Range
  - Without BIAS: 1.4 V to 6.5 V
  - With BIAS: 1.1 V to 6.5 V
- Output Voltage Options:
  - Fixed Output Voltage: 0.8 V to 3.95 V
  - Adjustable Output Voltage: 0.8 V to 5.2 V
- ±1% Output Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range With BIAS
- 3-A Maximum Output Current
- Low Dropout Voltage: 300 mV Maximum at 3 A
- High PSRR:
  - 65 dB at 1 kHz
  - 30 dB at 1 MHz
- 4-μV_{RMS}Output Voltage Noise
- Excellent Transient Response
- Enable and Adjustable Soft-Start Control
- Open-Drain Power-Good (PG) Output
- Stable with 22-μF or Greater Ceramic Output Capacitor
- Over-Current Protection
- Over-Temperature Protection
- Operating Temperature Range: –40°C to +125°C
- Package Options:
  - QFN3.5X3.5-20

Applications

- Wireless Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

Description

The TPL9308 is a 3-A high-current, 4-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulator with maximum 300-mV ultra-low dropout voltage at 3-A load condition. The TPL9308 supports both fixed output voltage ranging from 0.8 V to 3.95 V and adjustable output voltage ranging from 0.8 V to 5.2 V with an external resistor dividers.

Ultra-low noise, high PSRR, and high-output-current capabilities make the TPL9308 an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, or high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensure the TPL9308 an optimal power supply for the large-scale processors and digital loads, such as ASIC, FPGA, CPLD, and DSP.

The TPL9308 provides a 20-pin QFN3.5X3.5 package with guaranteed operating junction temperature ranging (T_J) from −40°C to +125°C.

Typical Application Circuit

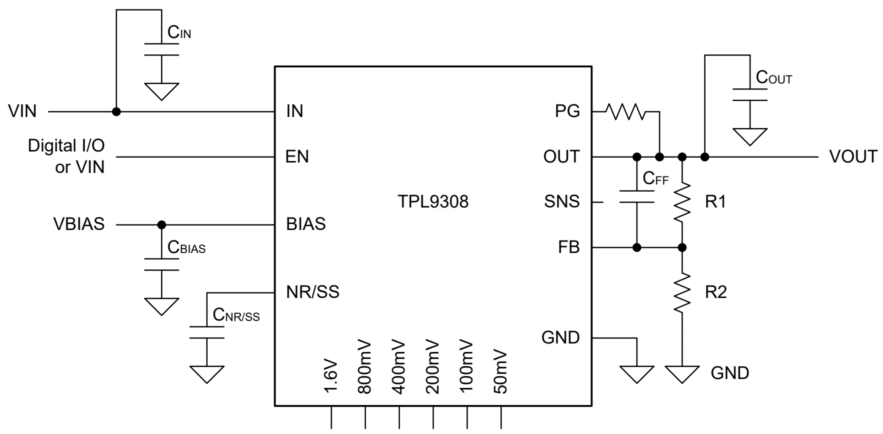


Table of Contents

Product Family Table

Order Number	Output Voltage (V)	Package
TPL9308AD-QF6R-S	Adjustable (0.8 V to 5.2 V)	QFN3.5X3.5-20

Revision History

Date	Revision	Notes
2023-01-15	Rev.Pre.0	Preliminary revision.
2023-02-28	Rev.A.0	Initial released.
2023-05-04	Rev.A.1	Updated Thermal Information.

Pin Configuration and Functions

TPL9308
QFN3.5X3.5-20 Package
Top View

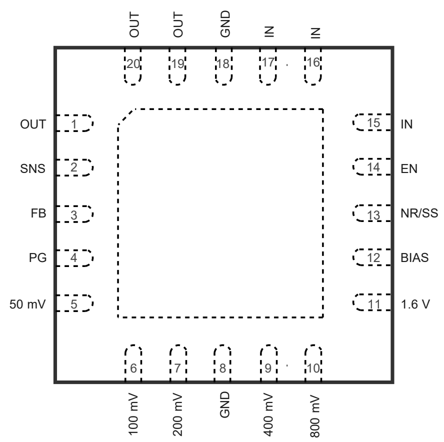


Table 1. Pin Functions: TPL9305

Pin No.	Pin Name	I/O	Description
5, 6, 7, 9, 10, 11	50mV, 100mV, 200mV, 400mV, 800mV, 1.6V	I	Fixed output voltage configuration pins. Connect these pins to ground to increase the output voltage. Leave these pins open when using the external resistor divider.
12	BIAS	I	BIAS input pin. A 10-μF capacitor or larger must be connected between this pin and ground. Leave BIAS pin open or tied to ground when not used.
14	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator.
3	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
8, 18	GND	–	Ground reference pin. Connect the GND pin to PCB ground plane directly.
15, 16, 17	IN	I	Input supply pin. A 10-μF or greater ceramic capacitor from IN to ground (as close as possible to IN pin) is required.
13	NR/SS	I	Noise-reduction and soft-start control pin. A 10-nF or greater capacitor from NR/SS to GND (as close as possible to NR/SS pin) is required.
1, 19, 20	OUT	O	Regulated output voltage pin. A 22-μF or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
4	PG	O	Open-drain power-good output pin. Leave the PG pin open when not used.
2	SNS	I	Output voltage sense input pin. Connect this pin to the load side of the output trace only when using the fixed output voltage. Leave this pin open when using the external resistor divider.

(1) Exposed PAD must be connected to a large-area ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
IN, BIAS, EN, PG		−0.3	7	V
OUT, SNS		−0.3	V_{IN} + 0.3	V
NR/SS, FB		−0.3	3.6	V
50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V		−0.3	V_{OUT} + 0.3	V
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
IN	Input Voltage	1.1		6.5	V
BIAS	BIAS Voltage	3		6.5	V
EN	Enable Voltage	0		6.5	V
OUT	Output Voltage	0.8		5.2	V
C_{IN}	Input Capacitor	10			μF
C_{OUT}	Output Capacitor	22	47		μF
$C_{NR/SS}$	NR/SS Capacitor		10	1000	nF
R_1	High-Side Resistor of the Resistor Divider		12.1		kΩ
R_2	Low-Side Resistor of the Resistor Divider			160	kΩ
R_{PG}	Power-good Pull-up Resistor	10		100	kΩ
T_J	Junction Temperature Range	−40		125	°C

Thermal Information

Package Type	$θ_{JA}$	$θ_{JB}$	$θ_{JC,TOP}$	$θ_{JC,BOTTOM}$	Unit
QFN3.5X3.5-20	30.8	10.1	39.1	3.2	°C/W

Electrical Characteristics

All test conditions: T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN} (1)	Input Supply Voltage Range		1.1		6.5	V
V_{BIAS}	Bias Supply Voltage Range	V_{IN} = 1.1 V	3		6.5	V
$UVLO_{IN1}$	Input Supply UVLO	V_{IN}rising with V_{BIAS} = 3 V			1.09	V
	Hysteresis			200		mV
$UVLO_{IN2}$	Input Supply UVLO	V_{IN} rising, V_{BIAS} = open			1.39	V
	Hysteresis			200		mV
$UVLO_{BIAS}$	BIAS Supply UVLO	V_{BIAS} rising, V_{IN} = 1.1 V			2.9	V
	Hysteresis			200		mV
I_{GND}	GND Pin Current	V_{IN} = 6.5 V, I_{OUT} = 5 mA		5	15	mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A		5	15	mA
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, I_{OUT} = 3 A		5	15	mA
I_{SD}	Shutdown Current	V_{IN} = 6.5 V, V_{EN} = 0.5 V, PG = open			68	µA
I_{BIAS}	BIAS Pin Current	V_{IN} = 1.1 V, V_{BIAS} = 6.5 V, I_{OUT} = 3 A		2.5	5	mA
Enable and Power Good						
$V_{IH(EN)}$	EN High-Level Input	Device enable	1.1		6.5	V
$V_{IL(EN)}$	EN Low-Level Input	Device disable	0		0.4	V
I_{EN}	EN Pin Current	V_{IN} = 6.5 V, V_{EN} = 0 V to 6.5 V	−0.5		0.5	µA
V_{PG}	PG Threshold	V_{OUT}falling	82%	84%	88%	× V_{OUT}
	Hysteresis			2%		× V_{OUT}
$V_{OL(PG)}$	PG Low-Level Output	V_{OUT} < V_{PG}, source 1 mA to PG pin			0.4	V
I_{PG}	PG Leakage Current	V_{OUT} > V_{PG}, apply 6.5 V at PG pin			1	µA

(1) Minimum V_{IN} = $V_{OUT(NOM)}$ + V_{DO} or 1.4 V or 1.1 V with V_{BIAS} = 3 V, whichever is greater.

Electrical Characteristics (Continued)

All test conditions: T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS}= open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = open, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

Parameter		Conditions		Min	Typ	Max	Unit
Regulated Output Voltage and Current							
VOUT	Output Voltage Range	Fixed		0.8		3.95	V
		Adjustable		0.8		5.2	V
	Accuracy [(1)]	V_{OUT} = 0.8 V to 5.2 V, I_{OUT} = 5 mA to 2 A		−1%		1%	
$ΔV_{OUT}$	Line Regulation	V_{IN} = 1.4 V to 6.5 V, I_{OUT} = 5 mA			0.03		mV/V
	Load Regulation	V_{IN} = 1.4 V, I_{OUT} = 5 mA to 2 A			0.7		mV/A
V_{FB}	Feedback Voltage				0.8		V
I_{FB}	FB Leakage Current	V_{IN} = 6.5 V, stress V_{FB} = 0.8 V		−100		100	nA
$V_{NR/SS}$	NR/SS Voltage				0.8		V
$I_{NR/SS}$	NR/SS Charging Current	V_{IN} = 6.5 V, $V_{NR/SS}$ = 0		6	7.8	9	µA
V_{DO}	Dropout Voltage	V_{IN} = 1.4 V, I_{OUT} = 1 A, V_{FB} = 0.8 V – 3%			40	100	mV
		V_{IN} = 1.4 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			80	200	mV
		V_{IN} = 1.4 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			120	300	mV
		V_{IN} = 5.6 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			120	300	mV
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, I_{OUT} = 1 A, V_{FB} = 0.8 V – 3%			40	100	mV
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, I_{OUT} = 2 A, V_{FB} = 0.8 V – 3%			80	200	mV
		V_{IN} = 1.1 V, V_{BIAS} = 3 V, I_{OUT} = 3 A, V_{FB} = 0.8 V – 3%			120	300	mV
I_{LIM}	Output Current Limit	V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{OUT} is forced at 90% × $V_{OUT(NOM)}$		3.7	4.7		A
I_{SC}	Short-Circuit Current Limit	R_{LOAD} ≤ 20 mΩ			1.5		A
PSRR and Noise							
PSRR	Power Supply Ripple Rejection	I_{OUT} = 3 A, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF	f = 1 kHz		65		dB
			f = 1 MHz		30		dB
			f = 1 kHz, V_{BIAS} = 3 V		65		dB
			f = 1 MHz, V_{BIAS} = 3 V		30		dB

(1) Resistor tolerances are not included. The device is not tested under conditions where V_{IN} > V_{OUT} + 2.5 V and I_{OUT} = 2 A because the power dissipation is higher than the maximum rating of the package.

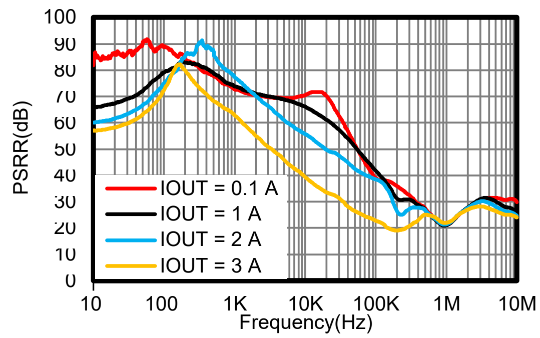
Electrical Characteristics (Continued)

All test conditions: T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS}= open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 μF, C_{OUT} = 22 μF, $C_{NR/SS}$ = 0 nF, C_{FF} = open, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
PSRR and Noise						
V_N	Output Noise Voltage	BW = 10 Hz to 100 kHz, V_{IN} = 1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.8 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 22 μF		4		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{IN} = 5.4 V V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 100 nF, C_{OUT} = 22 μF		8		μV_{RMS}
		BW = 10 Hz to 100 kHz, V_{IN} = 5.4 V V_{OUT} = 5 V, I_{OUT} = 3 A, $C_{NR/SS}$ = 100 nF, C_{FF} = 10 nF, C_{OUT} = 22 μF		10		μV_{RMS}
Temperature Range						
T_{SD}	Thermal Shutdown Threshold	Temperature increasing		160		°C
	Hysteresis			20		°C
T_J	Operating Temperature		−40		125	°C

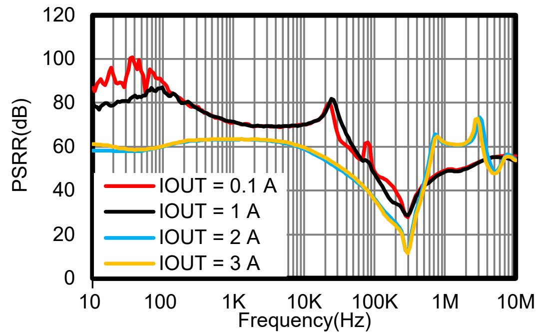
Typical Performance Characteristics

All test conditions: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.4 V or 1.4 V, whichever is greater; V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.8 V, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, OUT connect to 50 Ω to ground, PG connected to 100 kΩ to OUT, unless otherwise noted.



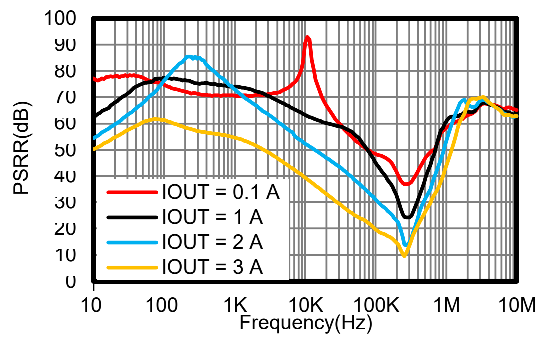
V_{IN} = 1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.8 V, C_{IN} = 10 µF, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 1. V_{IN} PSRR



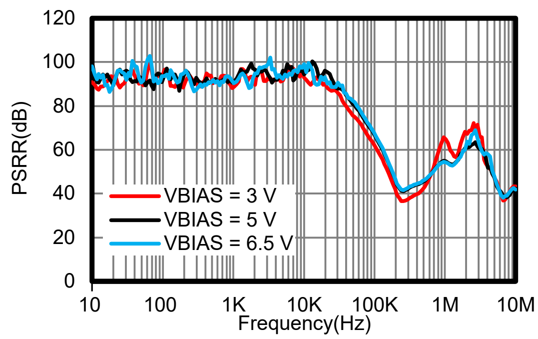
V_{IN} = 1.1 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V

Figure 2. V_{IN} PSRR



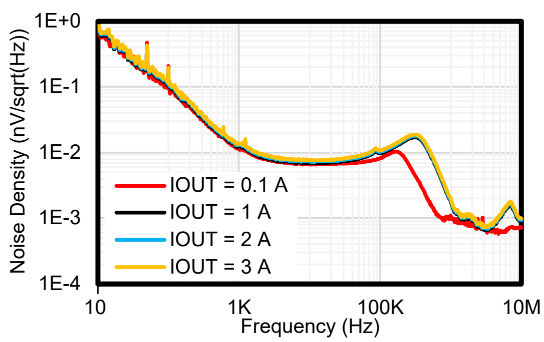
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, C_{IN} = 10 µF, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 3. V_{IN} PSRR



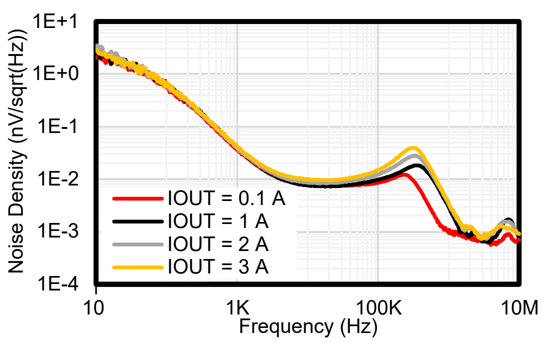
V_{IN} = 1.1 V, V_{OUT} = 0.8 V, C_{IN} = 10 µF, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 4. V_{BIAS} PSRR



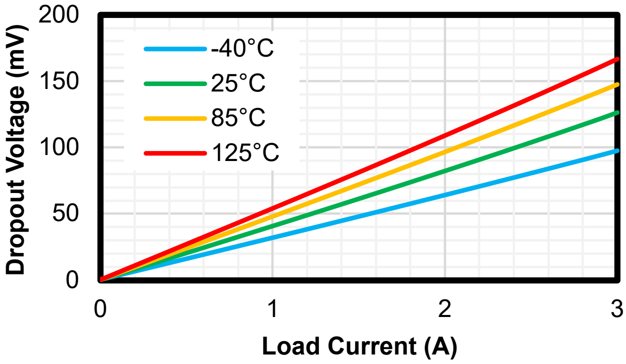
V_{IN} = 1.4 V, V_{OUT} = 0.8 V, C_{IN} = 10 µF, C_{OUT} = 47 µF || 10 µF || 10 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 5. Noise



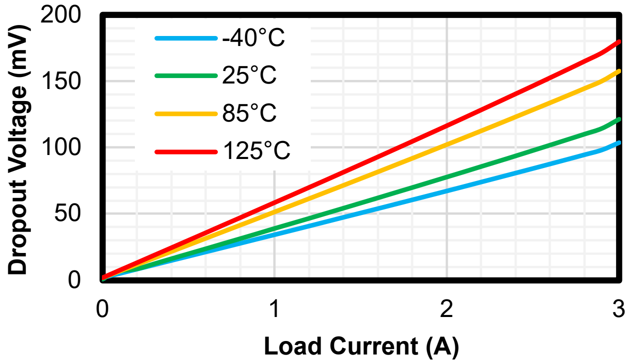
V_{IN} = 5.5 V, V_{OUT} = 5.2 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 6. Noise



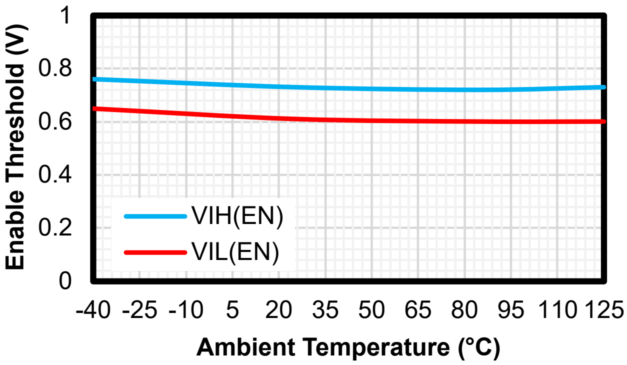
V_{IN} = 1.4 V

Figure 7. Dropout Voltage vs. Output Current



V_{IN} = 5.5 V

Figure 8. Dropout Voltage vs Output Current



V_{IN} = 1.4 V

Figure 9. Enable Threshold vs. Temperature

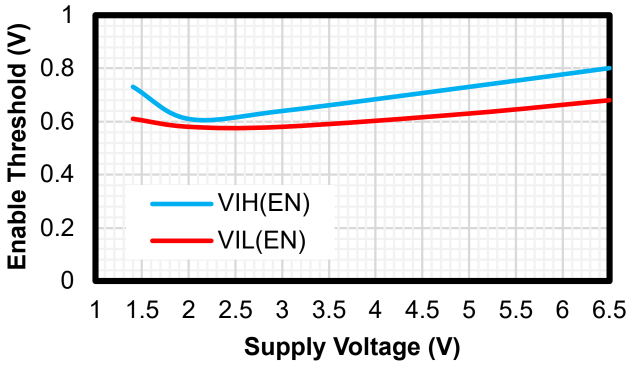
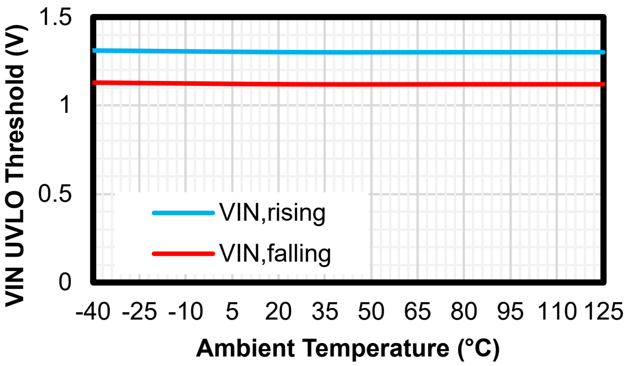
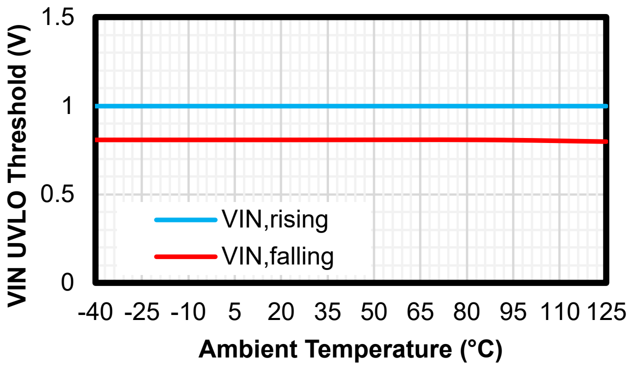


Figure 10. Enable Threshold vs Input Voltage



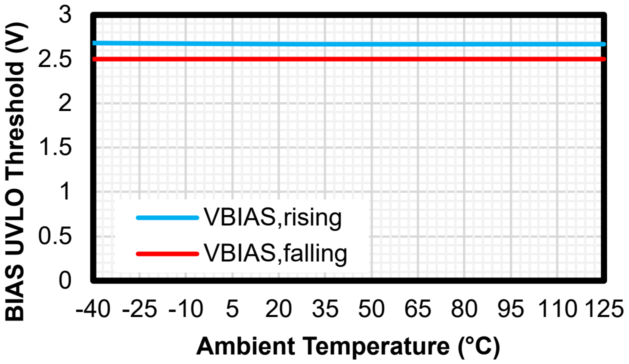
Without V_{BIAS}

Figure 11. VIN UVLO vs. Temperature



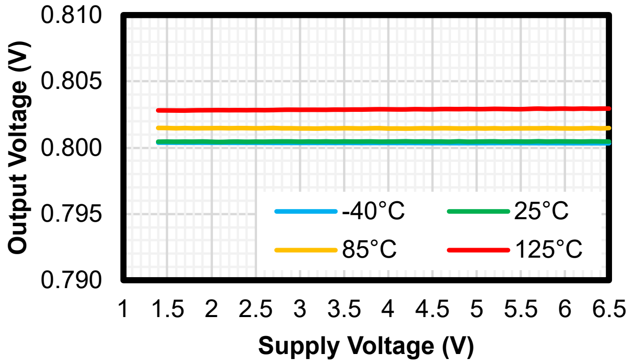
With V_{BIAS} = 3 V

Figure 12. VIN UVLO vs. Temperature



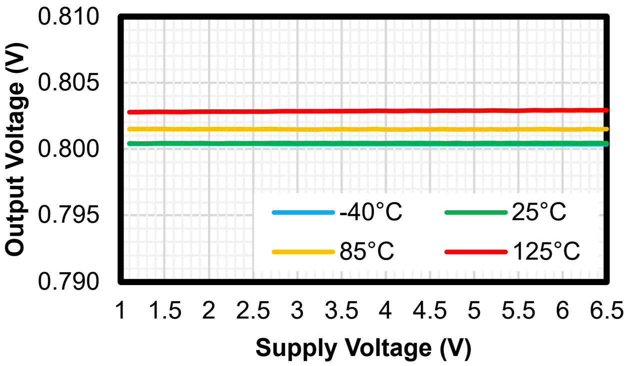
With V_{IN} = 1.1 V

Figure 13. BIAS UVLO vs. Temperature



Without V_{BIAS}

Figure 14. Line Regulation



With V_{BIAS} = 3 V

Figure 15. Line Regulation

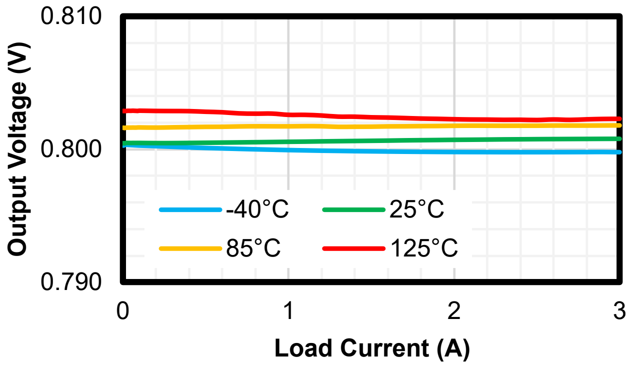
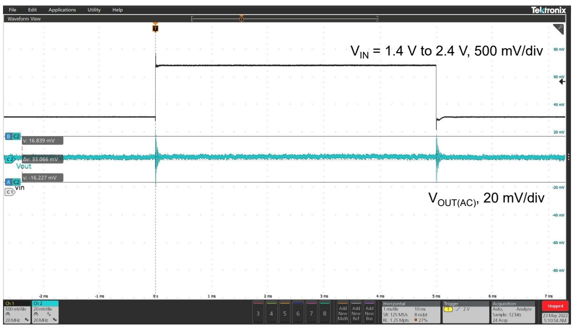
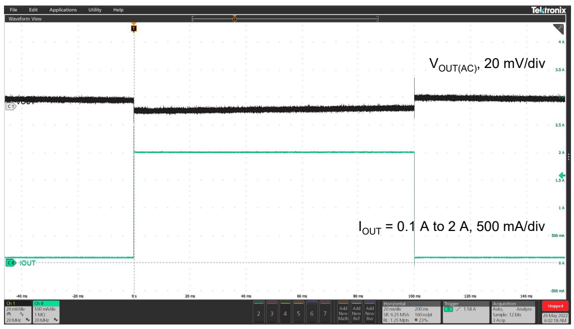


Figure 16. Load Regulation



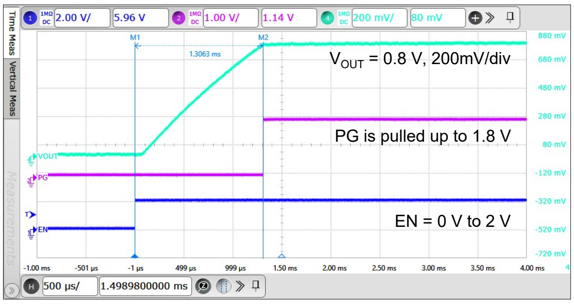
V_{IN} = 1.4 V to 2.4 V, V_{OUT} = 0.8 V, I_{OUT} = 1 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 17. Line Transient



V_{IN} = 1.4 V, V_{OUT} = 0.8 V, I_{OUT} = 0.1 A to 2 A, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF

Figure 18. Load Transient



V_{IN} = 1.4 V, V_{OUT} = 0.8 V, C_{OUT} = 22 µF, $C_{NR/SS}$ = 10 nF, no load

Figure 19. Startup

Detailed Description

Overview

The TPL9308 is a 3-A high-current, 4-μV_{RMS} low-noise, high-PSRR, high-accuracy linear regulators with maximum 300-mV ultra-low dropout voltage at 3-A load condition. The TPL9308 supports both fixed output voltage ranging from 0.8 V to 3.95 V and adjustable output voltage ranging from 0.8 V to 5.2 V with an external resistor divider.

Ultra-low noise, high-PSRR, and high-output-current capabilities make the TPL9308 an ideal power supply for noise-sensitive applications, such as high-speed communication facilities, test and measurement devices, and high-definition imaging equipment. Accurate output voltage tolerance, output voltage remote sensing, excellent transient response, and adjustable soft-start control ensures the TPL9308 an optimal power supply for large-scale processors and digital loads, such as CPU, ASIC, FPGA, CPLD, and DSP.

Functional Block Diagram

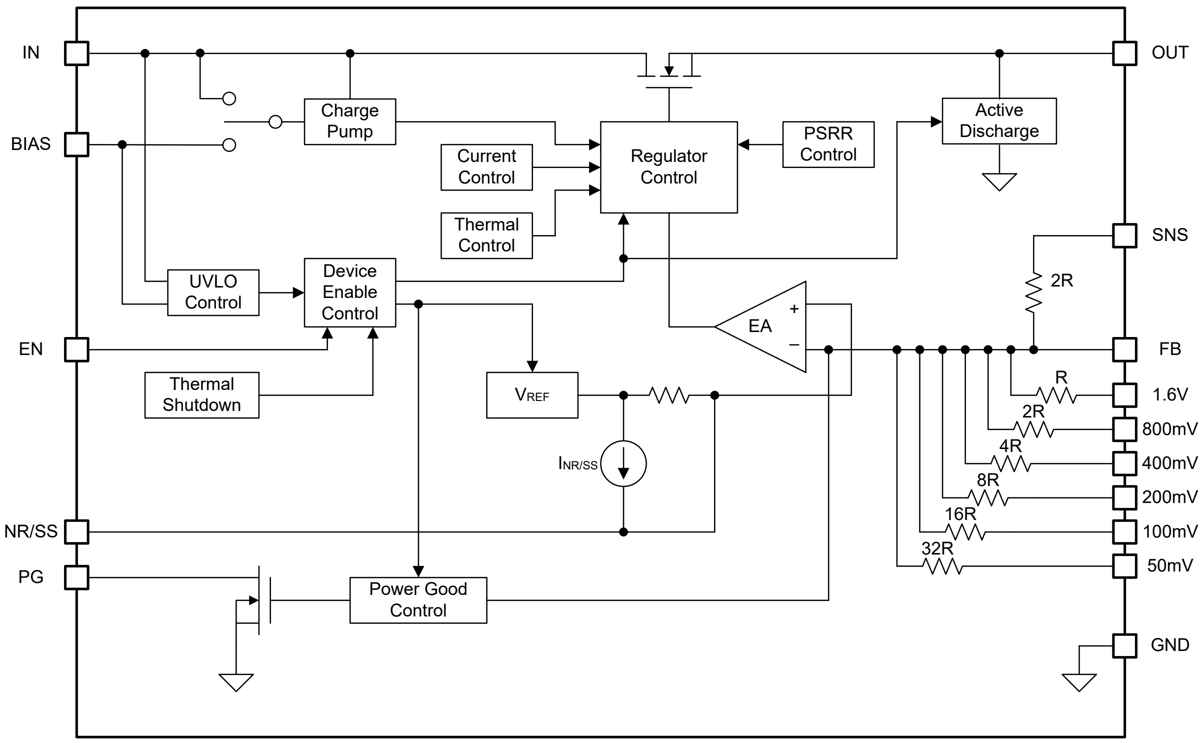


Figure 20. Functional Block Diagram

Feature Description

Enable (EN)

The TPL9308 provides a device with an enable pin (EN) to enable or disable the device. Connect the enable pin to the GPIO of an external digital logic control circuit to control the device. When the V_{EN} voltage falls below $V_{IL(EN)}$, the LDO device turns off, and when the V_{EN} ramps above $V_{IH(EN)}$, the LDO device turns on.

The TPL9308 also integrates an active discharge function. During normal operation, when the enable pin is pulled down below $V_{IL(EN)}$, the output voltage is discharged through the internal resistive path.

Under-Voltage Lockout (UVLO)

The TPL9308 uses an under-voltage lockout circuit to keep the output shut-off until the internal circuitry operates properly.

Voltage Regulation (OUT, FB)

The TPL9308 provides two options to set the output voltages: fixed output voltage configured by the programming pins or adjustable output voltage by external resistors.

Fixed Output Voltage Setting

The TPL9308 integrates resistor dividers internally to set the fixed output voltage. The fixed output voltage can be set from 0.8 V to 3.95 V by connecting the output voltage setting pins (pin 5 to pin 11) to ground or leaving them open. Use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{NR/SS} + V_{Pin\_Setting} \quad (1)$$

Table 2 provides a full list of different output voltage targets and the corresponding pin settings.

Table 2. Fixed Output Voltage Setting

V_{OUT} (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V	VOUT (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
Pin	5	6	7	9	10	11	Pin	5	6	7	9	10	11
0.80	Open	Open	Open	Open	Open	Open	2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open	2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND
1.00	Open	Open	GND	Open	Open	Open	2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open	2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open	2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open	2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open	3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open	3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open	3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open	3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open	3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open	3.50	Open	GND	GND	Open	GND	GND

1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open	3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open	3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open	3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open	3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

Table 3. External Resistor Combinations

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.80	0	Open	0.800
0.81	2	160	0.810
0.82	4.02	160	0.820
0.83	6.04	160	0.830
0.84	8.06	160	0.840
0.85	10	160	0.850
0.86	12	160	0.860
0.87	12.4	143	0.869
0.88	12.4	124	0.880
0.89	12	107	0.890
0.90	12.4	100	0.899
0.95	12.4	66.5	0.949
1.00	12.4	49.9	0.999
1.10	12.4	33.2	1.099
1.20	12.4	24.9	1.198
1.50	12.4	14.3	1.494
1.80	12.4	10	1.792
1.90	12.1	8.87	1.891
2.50	12.4	5.9	2.481
2.85	12.1	4.75	2.838
3.00	12.1	4.42	2.990
3.30	11.8	3.74	3.324
3.60	12.1	3.48	3.582
4.50	11.8	2.55	4.502
5.00	12.4	2.37	4.986

Adjustable Output Voltage Setting

The TPL9308 also provides an adjustable output voltage option. Using external resistor dividers, the output voltage of TPL9308 is determined by the value of the resistors R1 and R2 in Figure 21. Use the Equation 2 to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Where,

- the feedback voltage V_{FB} is 0.8 V.
- R1 is the high-side feedback resistor.
- R2 is the low-side feedback resistor.

Table 3 provides a list of recommended resistor combinations to achieve the common output voltage values.

Output Soft-Start Control (NR/SS)

The TPL9308 integrates an adjustable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin ($C_{NR/SS}$), the output start-up time can be calculated with Equation 3.

$$t_{STRATUP} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (3)$$

Where,

- the typical value of $V_{NR/SS}$ is 0.8 V.
- the typical value of $I_{NR/SS}$ is 7.8 μA.
- $C_{NR/SS}$ is the external capacitor at the NR/SS pin.

Charge Pump Noise

The TPL9308 integrates a charge pump to improve the PSRR and transient response under low input voltage conditions. The charge pump circuit generates a minimal amount of noise at the frequency of around 15 MHz. It is recommended to use 10-nF to 100-nF bypass capacitors close to the load a ferrite bead between the LDO output and the load input capacitors, forming a pi-filter to reduce the high-frequency noise level.

Power Good (PG)

The TPL9308 integrates an open-drain output power good indicator. Connect the PG pin to a pull-up voltage through a resistor from 10 kΩ to 100 kΩ if the power good function is used. Left the PG pin open if it is not used.

After regulator startup, the PG pin keeps low impendence until the output voltage reaches the power good threshold $V_{PG,TH}$. When the output voltage is higher than $V_{PG,TH}$, the PG pin turns to high output impedance, and PG is pulled up to a high voltage level to indicate the output voltage is ready.

Output Active Discharge

The TPL9308 integrates an output discharge path from OUT to GND. When the device is disabled, the output will actively discharge the output voltage through an internal resistor of several hundred ohms.

Do not rely on this active discharge circuit for discharging large output capacitors when the input voltage falls below the output voltage. Reverse current flow through internal power MOSFET can permanently damage the device, and external current protection is essential in this condition.

Over-Current Protection and Short-to-Ground Protection

The TPL9308 integrates an internal current limit that helps to protect the device during fault conditions.

- When the output is pulled down below the target output voltage, over-current protection starts to work and limit the output current to a typical value of 4.7 A.
- When the output is shorted to ground directly, short-to-ground protection starts to work and limit the output current to I_{SC}.

Under over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause over-temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is from −40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but will reduce the device lifetime for long-term use.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. When the device cools down and the junction temperature falls below the value, which equals to thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL9308 is a 3-A high-current, low-noise, high-PSRR, high-accuracy linear regulators with a maximum 300-mV ultra-low dropout voltage at 3-A load condition. The following application schematics show the typical usage of the TPL9308.

Typical Application

Adjustable Output Operation

Figure 21 shows a typical application schematic of the TPL9308 with adjustable output operation. Refer to section Adjustable Output Voltage Setting to set the output voltage.

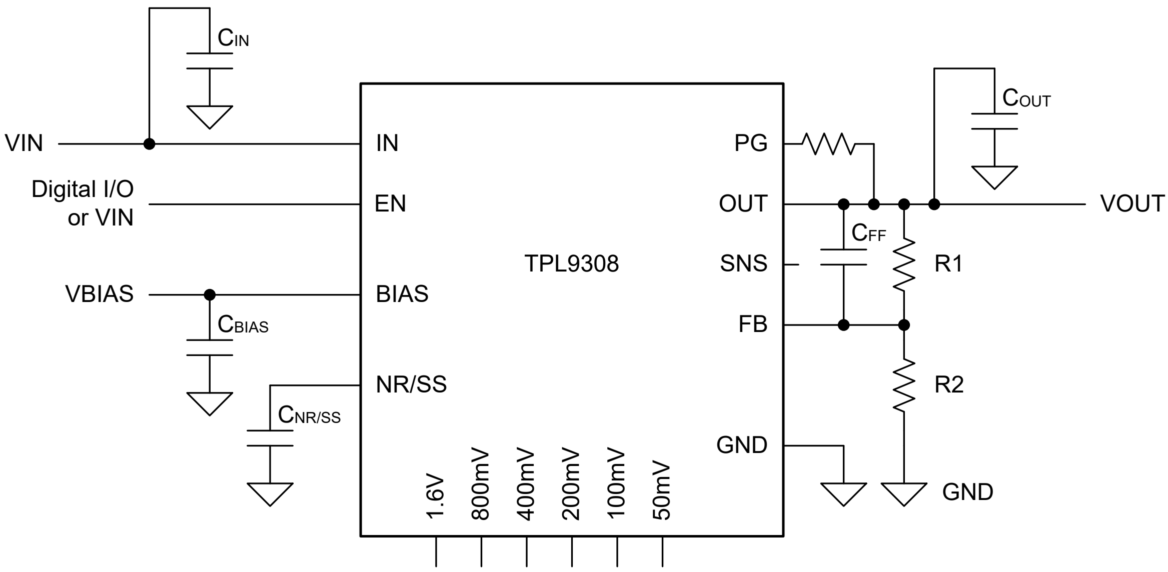


Figure 21. Adjustable Output Operation

Fixed Output Operation

Figure 22 shows a typical application schematic of the TPL9308 with fixed output operation. Refer to the section Fixed Output Voltage Settingto set the output voltage. In this example, output voltage is set to 1.8 V ($V_{NR/SS}$+ 0.8 V + 0.2 V).

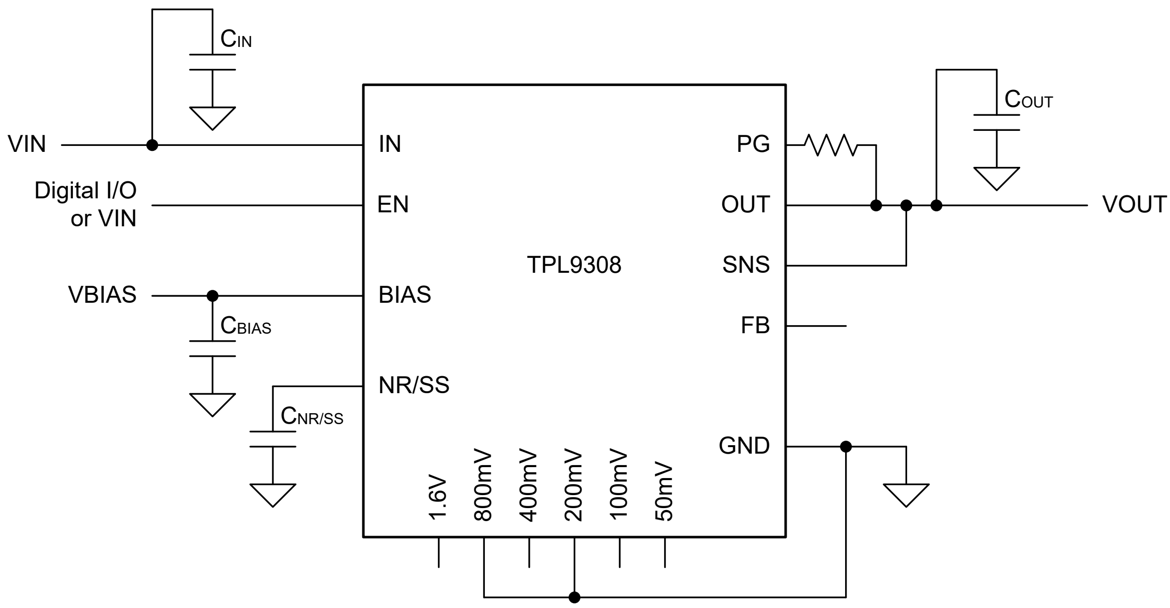


Figure 22. Fixed 1.8-V Output with QFN Package

Input Capacitor and Output Capacitor

The TPL9308 is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperature ranges.

3PEAK recommends adding a 10-μF or greater capacitor with a 0.1-μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL9308 requires a 22-μF or greater output capacitor. 3PEAK recommends selecting an X7R-type 47-μF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 4 .

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (4)$$

The junction temperature can be estimated using Equation 5. θ_{JA} is the junction-to-ambient thermal resistance.

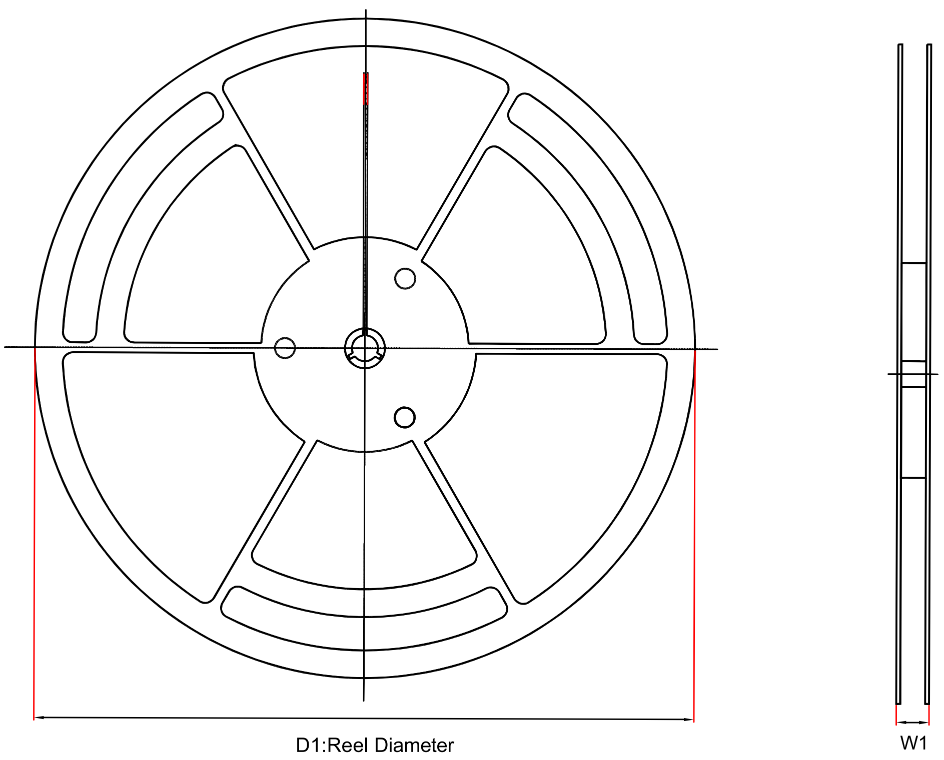
$$T_J = T_A + P_D \times \theta_{JA} \quad (5)$$

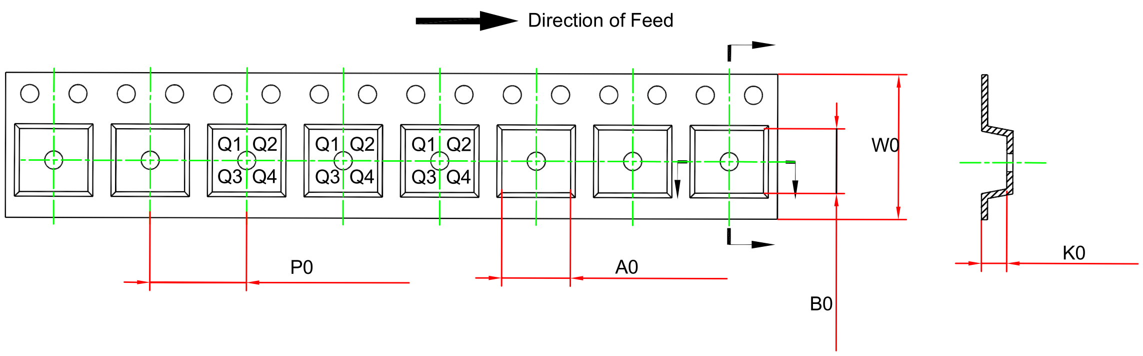
Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible, and the vias between capacitors and device power pins must be avoided.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Tape and Reel Information



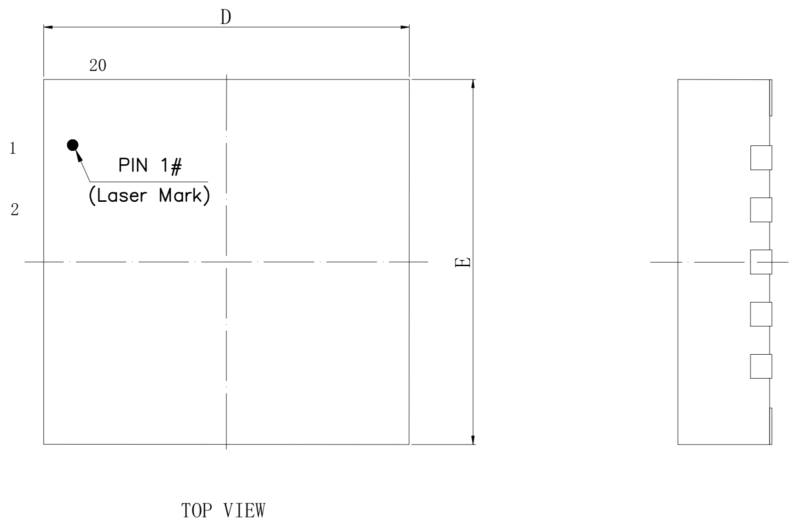


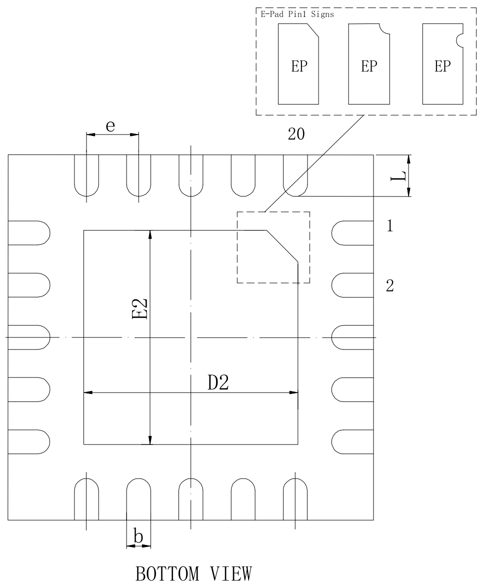
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL9308AD-QF6R-S	QFN3.5X3.5-20	330	16.4	3.75	3.75	1.1	8	12	Q2

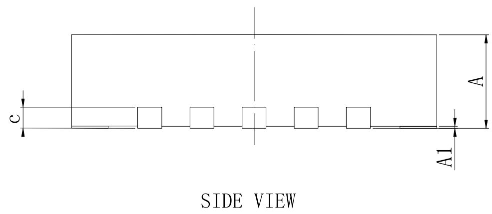
Package Outline Dimensions

QFN3.5X3.5-20

Package Outline Dimensions QF6(QFN3.5X3.5-20-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
c	0.203 REF		0.008 REF	
D	3.400	3.600	0.134	0.142
E	3.400	3.600	0.134	0.142
e	0.500 BSC		0.020 BSC	
L	0.250	0.450	0.010	0.018
D2	2.050	2.250	0.081	0.089
E2	2.050	2.250	0.081	0.089

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL9308AD-QF6R-S	−40°C to 125°C	QFN3.5X3.5-20	L938A	MSL3	Tape and Reel, 4,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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