Features

- SD 3.0 spec-compliant voltage translation to support SDR104 mode
- Supports high speed clock, up to 208 MHz
- 1.2 V to 1.8 V host side interface voltage support
- 100 mA peak current regulator to supply the card-side I/Os
- Low power consumption by push-pull output stage
- Automatic enable and disable through V_{SD}
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Package: WLCSP20; pitch 0.4 mm
- ESD Protection on card side
  - 8kV IEC61000-4-2, contact mode
  - 15kV IEC61000-4-2, air-discharge mode

Description

The TPT24857 is an SD 3.0 spec-compliant memory card voltage-level translator with bidirectional control. It is designed to translate voltage between voltage 1.8 V to 3.0 V in card side and 1.2 V to 1.8 V in host side.

The device supports SD 3.0 SDR104 in high speed mode, and covers down to SDR50, DDR50, SDR25, SDR12 & SD 2.0 (50 MHz and 25 MHz) modes. The TPT24857 has an integrated voltage regulator to supply the card-side I/Os, can support 100mA peak current with an auto-enable function. The device also has the EMI filters and support robust ESD protections: 10kV IEC contact ESD.

TPT24857 is available in WLCSP20 with 0.4mm pitch package, and is characterized from –40°C to +85°C.

Applications

- Smartphone
- Mobile handset and Digital camera
- Tablet PC/ Laptop
- SD, MMC or microSD card readers

Function block

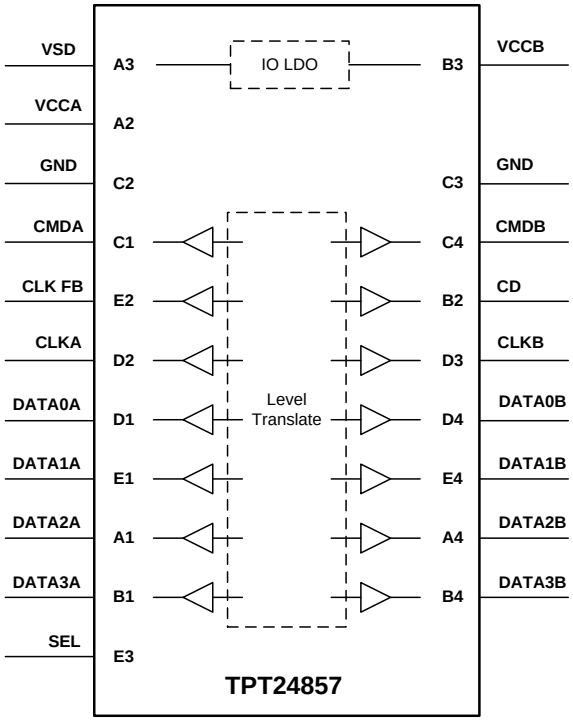


Table of Contents

Revision History

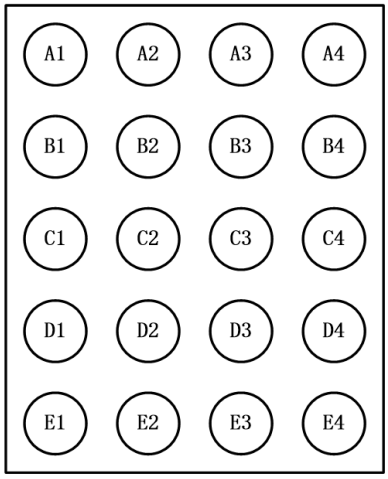
Date	Revision	Notes
2020/1/2	Rev. Pre 0.1	Initial Version
2020/2/21	Rev. Pre 0.2	Update MSL level 1 and ICCA current
2020/5/11	Rev. Pre 0.3	Update electrical parameter
2020/6/24	Rev. 0	Fix datasheet
2020/9/11	Rev. A0	Update host side and card side, min/max value of tr/tf

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT24857-WS8R-S	-40 to 85°C	WLCSP20	T27	MSL1	Tape and Reel, 3000

Pin Configuration and Functions

TPT24857-WS8R
WLCSP20



TPT24857-WS8R
Pin Naming

DATA2A	VCCA	VSD	DATA2B
DATA3A	CD	VCCB	DATA3B
CDMA	GND	GND	CDMB
DATA0A	CLKA	CLKB	DATA0B
DATA1A	CLK FB	SEL	DATA1B

Pin Functions

Pin name	Pin No	I/O	Description
DAT2A	A1	I/O	data 2 input or output on host side
VCCA	A2	-	supply voltage from host side
VSD	A3	-	supply voltage
DAT2B	A4	I/O	data 2 input or output on memory card side
DAT3A	B1	I/O	data 3 input or output on host side
CD	B2	O	card detect switch biasing output
VCCB	B3	-	internal supply decoupling (VLDO)
DAT3B	B4	I/O	data 3 input or output on memory card side
CMDA	C1	I/O	command input or output on host side
GND	C2	-	supply ground
GND	C3	-	supply ground
CMDB	C4	I/O	command input or output on memory card side
DAT0A	D1	I/O	data 0 input or output on host side
CLKA	D2	I	clock signal input on host side
CLKB	D3	O	clock signal output on memory card side
DAT0B	D4	I/O	data 0 input or output on memory card side
DAT1A	E1	I/O	data 1 input or output on host side
CLK_FB	E2	O	clock feedback output on host side
SEL	E3	I	card side I/O voltage level select
DAT1B	E4	I/O	data 1 input or output on memory card side

Absolute Maximum Ratings

Parameter		MIN	MAX	UNIT
VCCA	Host side reference voltage range	–0.5	5.5	V
VSD, VCCB	Power supply and Card side reference bias voltage range	–0.5	5.5	V
V_I	Input voltage range(2)	–0.5	5.5	V
Ptotal	Total power dissipation		1000	mW
	Peak current in card side		100	mA
$T_{j(max)}$	Maximum junction temperature		85	°C
T_{stg}	Storage temperature range	–65	150	°C

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
IEC-ESD	IEC-61000-4-2, Contact Discharge	Side B Pin	8	kV
	IEC-61000-4-2, Air-Gap Discharge	Side B Pin	15	kV
HBM	HBM per ANSI/ESDA/JEDEC JS-001	All pins	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV
Latch Up	Latch up per JESD78	All Pin	600	mA

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
V_{SD}	Supply voltage	2.9		3.6	V
V_{CCA}	Host side voltage	1.1		2.0	V
V_I	Input voltage in host side	-0.3		V_{CCA}+0.3	V
	Input voltage in card side	-0.3		V_{LDO}+0.3	V
Cap	External capacitance at pin VCCB		2.2		uF
	External capacitance at pin VSD		0.1		uF
	External capacitance at pin VCCA		0.1		uF
T_A	Operating ambient temperature	–40		85	°C

Integrated resistors

Table 1. T_A = 25°C

Symbol	Description	Min	Typ	Max	Unit
R_{pd}	VLDO pull-down resistor to GND	70	100	130	Ω
	SEL pull-down resistor to GND	210	350	550	kΩ
R_{pu}	Pull-up resistor at pins of data-x and CMDx	20	33	40	kΩ
	Pull-up resistor at CD pin to VCCA	70	100	130	kΩ
Rs	Series resistor at host side, tolerance ±30% [1]		22.5		Ω
	Series resistor at card side, tolerance ±30% [1]		15		Ω

[1] Rs is provided by design simulation

Device Function table

Table 2. SD card side voltage level control signal truth table

Input	Output		
SEL	VCCB	Pins	Function
H	1.8 V	DAT0B to DAT3B, CLKB, CMDB	low supply voltage level (1.8 V_{typ})
L	tracking V_{SD}	DAT0B to DAT3B, CLKB, CMDB	high supply voltage level (tracking V_{SD})

(1) H = HIGH; L = LOW; X = don't care

(2) Host-side pins are not influenced by SEL.

Electrical Characteristics

Typical test condition is VSD = 3.0V, T_A = -40 ~ +85°C

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Automatic enable feature: V_{SD}						
V_{SDen}	Device enable voltage level	VCCA >=1.0 V, VSD rising edge	2.25	2.45	2.65	V
$V_{SDdisable}$	Device disable voltage level	VCCA >=1.0 V, VSD falling edge	2.2	2.4	2.6	V
$\triangle V_{SDen}$	V_{SDen} hysteresis voltage		30		150	mV
Supply voltage regulator for card-side I/O pin: VCCB						
$V_{O(LDO)}$	Regulator/switch output voltage	SEL = LOW;3.0 V =< V_{SD} =< 3.6 V; I_O < 100 mA	V_{SD}-0.2	V_{SD}-0.1	V_{SD}	V
		SEL = HIGH; V_{SD} >= 2.9 V; I_O < 100 mA	1.7	1.8	1.95	V
$I_{O(LDO)}$	Regulator/switch output current				100	mA
Host-side input signals: CMDA and DAT0A to DAT3A, CLKA; 1.1 V =< VCCA =< 2.0 V						
V_{IH}	High-level input voltage	VCCA=1.1V and VCCA=2.0V	0.75 x VCCA		VCCA + 0.3	V
V_{IL}	Low-level input voltage	VCCA=1.1V and VCCA=2.0V	-0.3		0.25 x VCCA	V
Host-side control signals; 1.1 V =< VCCA =< 2.0 V						
SEL						
VIH	High-level input voltage	VCCA=1.1V and VCCA=2.0V	0.75 x VCCA		VCCA + 0.3	V
VIL	Low-level input voltage	VCCA=1.1V and VCCA=2.0V	-0.3		0.25 x VCCA	V
Host-side output signals: CLK_FB, CMDA and DAT0A to DAT3A; 1.1 V =< VCCA =< 2.0 V						
V_{OH}	High-level output voltage	I_O = 2 mA; V_I = V_{IH} (card side) for CLK_F	0.8 x VCCA			V
	High-level Output voltage	I_O = 2 μA; V_I = V_{IH} (card side) for CMDA, DATxA	0.8 x VCCA			V
V_{OL}	Low-level output voltage	I_O = -2 mA; V_I = V_{IL} (card side)			0.15 x VCCA	V
Card-side input signals: CMDB and DAT0B to DAT3B						
VIH	High-level input voltage	SEL = LOW (3.0 V card interface)	0.625 x $V_{O(LDO)}$	-	$V_{O(LDO)}$ + 0.3	V
		SEL = HIGH (1.8 V card interface)	0.625 x $V_{O(LDO)}$	-	$V_{O(LDO)}$ + 0.3	V
VIL	Low-level input voltage	SEL = LOW (3.0 V card interface)	-0.3	-	0.3 x $V_{O(LDO)}$	V
		SEL = HIGH (1.8 V card interface)	-0.3	-	0.35 x $V_{O(LDO)}$	V

[1] EMI filter line capacitance per data channel from I/O driver to pin;

Electrical Characteristics (Continue)

Typical test condition is VSD = 3.0V, T_A = -40 ~ +85°C

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Card-side output signal						
CMDB and DAT0B to DAT3B, CLKB						
V_{OH}	High-level output voltage for CLKB only	I_O = 4 mA; V_I = V_{IH} (host side); SEL = LOW (3.0 V card interface)	0.85 x $V_{O(LDO)}$	-	$V_{O(LDO)}$+0.3	V
		I_O = 2 mA; V_I = V_{IH} (host side); SEL = HIGH (1.8 V card interface)	0.85 x $V_{O(LDO)}$	-	2.0	V
	High-level output voltage for CMDB, DATxB	I_O = 2 µA; V_I = V_{IH} (host side); SEL = HIGH (1.8 V card interface)	0.85 x $V_{O(LDO)}$	-	2.0	V
V_{OL}	Low-level output voltage	I_O = -4 mA; V_I = V_{IL} (host side); SEL = LOW (2.9 V card interface)	-0.3	-	0.125 x $V_{O(LDO)}$	V
		I_O = -2 mA; V_I = $V_{I\ card\ L}$ (host side); SEL = HIGH (1.8 V interface)	-0.3	-	0.125x$V_{O(LDO)}$	V
Bus signal equivalent capacitance [1]						
C_{ch}	Channel capacitance	V_I = 0 V; f_i = 1 MHz; V_{SD} = 3.0 V; V_{CCA} = 1.8 V				
		host side		7		pF
		card side		15		pF
Current consumption						
$I_{CC(stat)}$	Static supply current	V_{SD} >= V_{SDen} (active mode); all inputs = HIGH;				
		SEL = LOW (3.0 V card interface)		72	110	uA
		SEL = HIGH (1.8 V card interface)		76	115	uA
$I_{CC(stb)}$	Standby supply current	VSD =< VSDen and VCCA =< 1.0 V (inactive mode); all host side inputs = HIGH				
		SEL = LOW (3.0 V card interface)		6	14	uA
		SEL = HIGH (1.8 V card interface)		6	14	uA

[1] EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is provided by design simulation

Switching Characteristics AC Performance

Voltage regulator, typical test condition is VSD = 3.0V, T_A = 25°C

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Voltage regulator output pin: V_{CCB}						
$t_{startup(LDO)}$	Regulator start-up time	V_{CCA} = 1.8 V; V_{SD} = 3.0 V; C_{ext} = 2.2 uF; see Figure			400	us
$t_{f(o)}$	Output fall time	$V_{O(LDO)}$ = 3.0 V to 1.8 V; SEL = LOW to HIGH; see Figure			1	ms
$t_{r(o)}$	Output rise time	$V_{O(LDO)}$ = 1.8 V to 3.0 V; SEL = HIGH to LOW; see Figure			100	us

Level translator

Typical test condition is VSD = 3.0V, T_A = 25°C

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Host side transition times						
t_r	rise time	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.8 V		0.4	-- [1]	ns
t_f	fall time			0.4	-- [1]	ns
t_r	rise time	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		0.4	-- [1]	ns
t_f	fall time			0.4	-- [1]	ns
Card side transition times						
t_r	rise time	SEL = HIGH (1.8 V card interface);	-- [2]	0.75	-- [2]	ns
t_f	fall time		-- [2]	0.75	-- [2]	ns
Card input transition times						
t_r	rise time	SEL = HIGH (1.8 V card interface); [1]	-- [3]	0.5	-- [3]	ns
t_f	fall time			0.45	-- [3]	ns
Host to card propoagation delay						
t_{pd1}	Propagation delay, DATxA to DATxB, CMDA to CMDB, CLKA to CLKB	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		3.75	-- [4]	ns
t_{pd2}	Propagation delay, CLKA to CLK_FB	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		6.5	-- [4]	ns
Card to host propagation delay						
t_{pd3}	Propagation delay, DATxB to DATxA, CMDB to CMDA	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		3.5	-- [4]	ns
Automatic Direction						
t_{dst}	Auto direction swapping time of data flow between from host to card and from card to host	SEL = HIGH (1.8 V card interface); V_{CCA} = 1.2 V		5	-- [5]	ns

[1] transition between VOL=0.35*V_{CCA} and VOH=0.65*V_{CCA}, tr max=1ns; tf max =1ns in lab test;

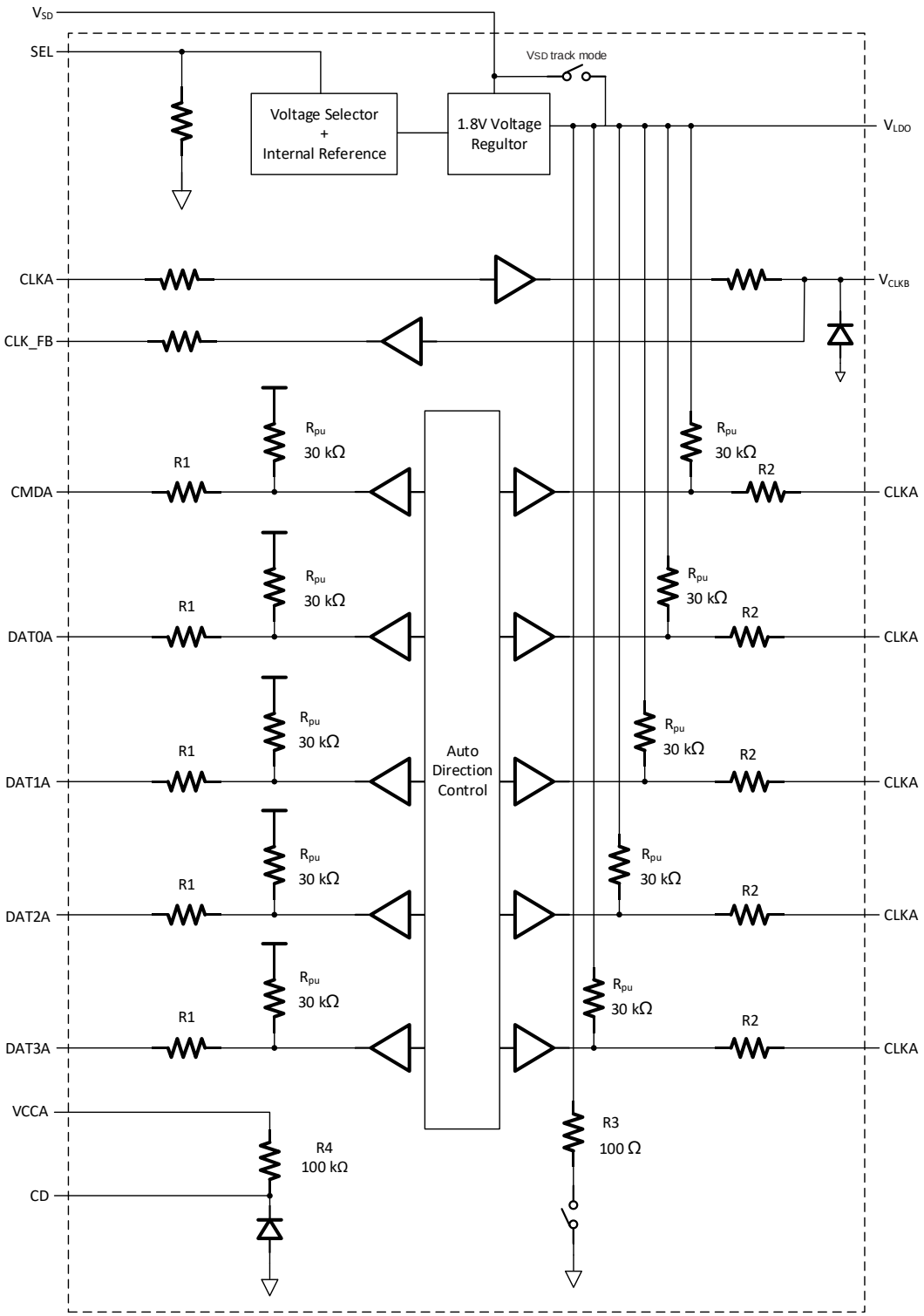
[2] transition between VOL=0.45V and VOH=1.4V, tr min=0.4ns; tf min =0.4ns; tr max=1.32ns; tf max =1.32ns in lab test;

[3] By design simulation, transition between VIL = 0.58 V and VIH = 1.27 V with Ctrace = 3.5 pF and Ccard+CRADLE = 12 pF, trace length =11 mm; tr min=0.2ns, tr max=0.96ns; tf max =0.96ns by design simulation;

[4] Parameters are provided by lab bench test, tpd1 max=6.5ns in lab test, tpd2 max = 15ns in lab test, tpd3 max=6.0ns in lab test

[5] By design simulation, tdst max =9.6ns;

Block Diagram



Function description

Enable and direction control

The device TPT24857 has an auto-enable feature. When V_{SD} rises above 2.65 V, the LDO and the level translator logic is enabled automatically. As soon as V_{SD} drops below the $V_{SDdisable}$, the LDO and the card side drivers and the level translator logic is disabled. All host side pins excluding CLKA are configured as inputs with a 30 kΩ resistor pulled up to V_{CCA}, refer to table 1.

Integrated voltage regulator

The low dropout voltage regulator delivers supply voltage for the voltage translators and the card-side input/output stages. It can support 1.8 V and 3.0 V signaling modes as required in the SD 3.0 specification. The switching time between the two output voltage modes is compliant with SD 3.0 specification. Depending on the signaling level at pin SEL, the regulator delivers 1.8 V (SEL = HIGH) or 3.0 V (SEL = LOW). See table 2 for the SD card side voltage level control signal truth table.

There is an external capacitor between the regulator output pin VCCB and ground for proper operation of the integrated voltage regulator. See table 1 for equivalent series resistance, and recommended capacitance in the table of Recommended Operating Conditions. It is recommended to place the capacitor close to the VSD and VCCB pin and also maintain short connections of both to the ground.

Feedback clock channel

The clock is transmitted from the host side to the SD card side, and the voltage translator and the PCB traces have some delay. It reduces timing margin for data read back from SD card, especially at higher data rate. In real case the clock is always delivered by the host, while the data in the timing critical read mode comes from the card， so there will be a feedback path provided to compensate the delay. That's why we need the feedback clock channel here.

EMI filter

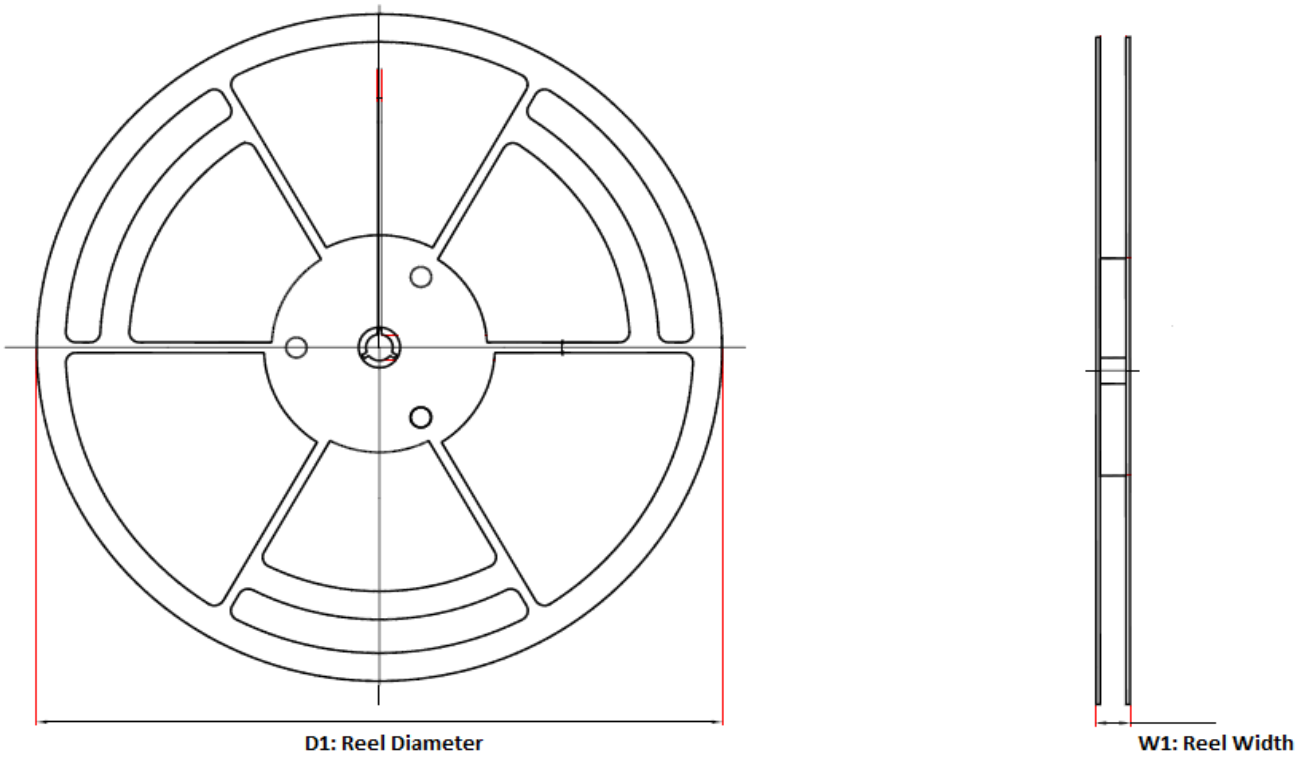
In the sensitive mobile application, the high speed communication is very complicated, then all input/output driver stages must be designed with EMI filters to reduce interferences.

ESD protection

The device TPT24857 has robust ESD protections on all SD card pins as well as on the VSD pin. The architecture prevents any stress for the host: the voltage translator discharges any stress through the supply ground.

Pin Card Detection (CD) might be pulled down by the SD card which has to be detected by the host. The pin is designed with International Electrotechnical Commission (IEC) system-level ESD protection and pull-up resistor connected to the host supply V_{CCA}.

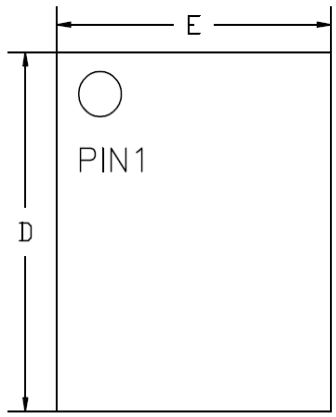
Tape and Reel Information



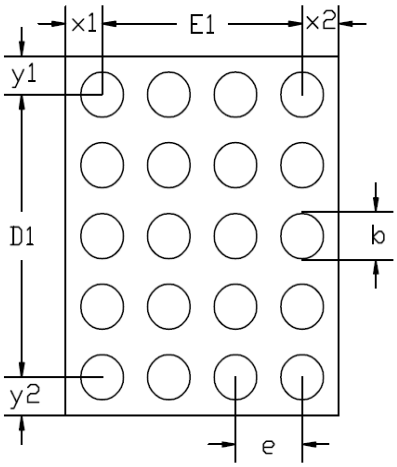
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT24857-WS8R-S	WLCSP20	Φ180	12	1.75	2.30	0.75	4	8	Q1

Package Outline Dimensions

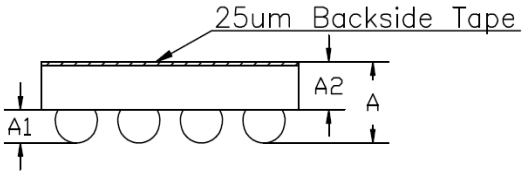
WS8R (WLCSP20)



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.445	0.490	0.535
A1	0.180	0.200	0.220
A2	0.265	0.290	0.315
D	2.010	2.040	2.070
D1	1.600BSC		
E	1.610	1.640	1.670
E1	1.200BSC		
b	0.230	0.260	0.290
e	0.400BSC		
x1	0.220 REF		
x2	0.220 REF		
y1	0.220 REF		
y2	0.220 REF		

IMPORTANT NOTICE AND DISCLAIMER

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.