

Features

- Exceeds the LVDS Standard TIA/EIA-644 for High speed Data Interchange
- Low-Voltage Differential 100-Ω (typical) Line Receivers for Signaling Rates, Up to 400 Mbps, 200Mbps Clock
- 3.3-V Power Supply Design
- 6 ns Maximum Propagation Delay
- 0.1 ns Differential Skew (Typical)
- Accepts Small Swing (350 mV Typical) VID Supports Open, Short, and Terminated Input Fail-Safe
- Power Down High Impedance on LVDS Inputs
- Bus-Pin Protection: ±8 kV HBM model
- -40°C to 85°C Operation Temperature Range

Description

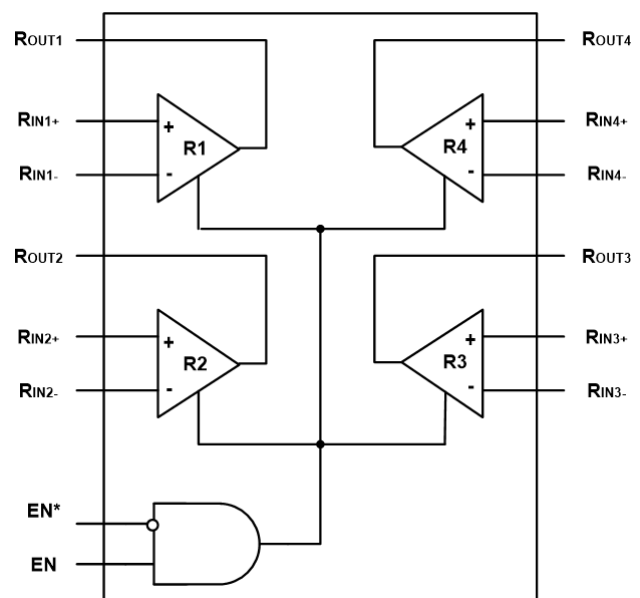
The TPT9L484 is a 3.3V 4-CH Low-Voltage Differential (LVDS) line receivers, which can support 400 Mbps data rates. Receiver inputs are protected against ±8kV ESD strikes without latch-up.

The TPT9L484 can accept low voltage differential input signals as 350 mV typical, and translates them to 3.3V CMOS output levels. The receivers support a Tri-state function that may be used to multi-channel outputs. The receivers also support open, shorted, and terminated (100 Ω) input Fail-safe, with holding output as HIGH level. The device is characterized for operation from -40°C to 85°C. The device is available in 16-lead TSSOP package.

Applications

- Backplane Multipoint Data/Clock Transmission
- Cellular Base Stations
- Network Switches and Routers
- Industrial Control
- Communication Infrastructure

Simplified Schematic



Revision History

Date	Revision	Notes
2018/12/14	Rev. Pre 0	Definition Draft
2019/02/26	Rev. Pre 0.1	Add package information
2019/06/06	Rev. Pre 0.2	Add Electrical data
2019/08/12	Rev. Pre 0.3	Update Electrical data
2019/08/23	Rev. Pre 0.4	Update Package information
2019/10/09	Rev. 0	Final version Rev. 0
2020/1/4	Rev. A	Update block diagram and Pin Functions

Order Information

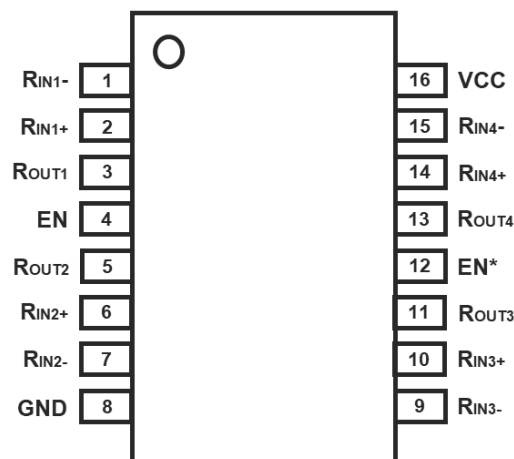
Mode Name	Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT9L484	TPT9L484L1-TSR-S	-40 to 85°C	16-Pin TSSOP	T9L484	MSL1	Tape and Reel, 3000

Mark Definition:

Include symbol, part, date code (detail to how to read date code), filled by OP

Pin Configuration and Functions

**TPT9L484L1-TSR
TSSOP16**



Pin Functions:

Pin No.	Pin Name	I/O	Description
1	RIN1-	Bus Input	Inverting receiver input pin
2	RIN1+	Bus Input	Noninverting receiver input pin
3	ROUT1	Output	Receiver output pin
4	EN	Input	Active high enable pin, see details in Truth Table
5	ROUT2	Output	Receiver output pin
6	RIN2+	Bus Input	Noninverting receiver input pin
7	RIN2-	Bus Input	Inverting receiver input pin
8	GND	Ground	Ground
9	RIN3-	Bus Input	Inverting receiver input pin
10	RIN3+	Bus Input	Noninverting receiver input pin
11	ROUT3	Output	Receiver output pin
12	EN*	Input	Active low enable pin, see details in Truth Table
13	ROUT4	Output	Receiver output pin
14	RIN4+	Bus Input	Noninverting receiver input pin
15	RIN4-	Bus Input	Inverting receiver input pin
16	VCC	Power	Power Supply

Function Table

Truth Table

Enable		Inputs	Outputs
EN	EN*	RIN+ - RIN-	ROUT
L	H	X	Z
All other combinations of Enable inputs $VID \geq 0.1\text{ V}$ H $VID \leq -0.1\text{ V}$ L Full Fail-safe OPEN/SHORT or Terminated H		$VID \geq 0.1\text{ V}$	H
		$VID \leq -0.1\text{ V}$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply voltage	V _{CC}	-0.3	4	V
Input voltage	R _{IN+} , R _{IN-}	-0.3	3.9	V
Enable input voltage	EN, EN*	-0.3	V _{CC} + 0.3	V
Output voltage	R _{OUT}	-0.3	V _{CC} + 0.3	V
Lead temperature, soldering (4 s)			260	°C
Maximum junction temperature, T _J			150	°C
Storage temperature, T _{stg}		-65	150	°C

ESD Rating

		Value	Unit
Human Body Model, per ANSI/ESDA/JEDEC JS-001	Bus Pin	8	kV
	All Pin Except Bus Pin	4	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	1	kV
IEC-61000-4-4, EFT, Bus Pins	Bus Pin	2	kV

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
16-Pin TSSOP	120	60	°C/W

Recommended Operation Conditions

		Min	Typ	Max	Unit
V _{CC}	Supply voltage	3	3.3	3.6	V
V _{IH}	High-level input voltage	2		V _{CC}	V
V _{IL}	Low-level input voltage	GND		0.8	V
V _{ID}	Magnitude of differential input voltage	GND		V _{CC}	V
T _A	Operating free-air temperature	-40	25	85	°C

Electrical Characteristics – DC Parameter

All test condition is $V_{CC} = 3.0$ to $3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{TH}	Differential input high threshold	$V_{CM} = 1.2 V, R_{IN+}, R_{IN-} \text{ pin}(2)$		25	100	mV
V_{TL}	Differential input low threshold		-100	-25		mV
V_{CMR}	Common mode voltage range	$V_{ID} = 200 \text{ mV peak to peak}, R_{IN+}, R_{IN-} \text{ pin}(3)$	0.1		2.3	V
I_{IN}	Input current	$V_{CC} = 3.6 V$ or $0 V,$ $R_{IN+}, R_{IN-} \text{ pin}$ $V_{IN} = 2.8 V$		-15	15	μA
		$V_{IN} = 0 V$		-15	15	μA
		$V_{CC} = 0 V, V_{IN} = 3.6 V, R_{IN+}, R_{IN-} \text{ pin}$	-20	12.5	20	μA
V_{OH}	Output high voltage	$I_{OH} = -0.4 \text{ mA}, V_{ID} = 200 \text{ mV}, R_{OUT} \text{ pin}$	2.7	3.3		V
		$I_{OH} = -0.4 \text{ mA},$ input terminated, $R_{OUT} \text{ pin}$	2.7	3.3		V
		$I_{OH} = -0.4 \text{ mA},$ input shorted, $R_{OUT} \text{ pin}$	2.7	3.3		V
V_{OL}	Output low voltage	$I_{OL} = 2 \text{ mA}, V_{ID} = -200 \text{ mV}, R_{OUT} \text{ pin}$		0.1	0.25	V
I_{OS}	Output short-circuit current	Enabled, $V_{OUT} = 0 V, R_{OUT} \text{ pin}(4)$	-15	-80	-120	mA
I_{OZ}	Output TRI-STATE current	Disabled, $V_{OUT} = 0 V$ or V_{CC}	-10	± 0.1	10	μA
V_{IH}	Input high voltage	EN, EN* pins		2	V_{CC}	V
V_{IL}	Input low voltage	EN, EN* pins	GND		0.8	V
I_I	Input current	$V_{IN} = 0 V$ or V_{CC} , other input = V_{CC} or GND, EN, EN* pins	-10		10	μA
V_{CL}	Input clamp voltage	$I_{CL} = -18 \text{ mA},$ EN, EN* pins		-0.8		V
I_{CC}	No load supply current	EN, EN* = V_{CC} or GND, inputs open, $V_{CC} \text{ pin}$		15	20	mA
	Receivers enabled	EN, EN* = $2.4 V$ or $0.5 V,$ inputs open, $V_{CC} \text{ pin}$		15	20	mA
I_{CCZ}	No load supply current	Receivers disabled, EN = GND, EN* = V_{CC} , inputs open, $V_{CC} \text{ pin}$		6	10	mA

Electrical Characteristics – AC Parameter

All test condition is $V_{CC} = 3.0$ to $3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PHL}	Differential propagation delay, high to low ⁽¹⁾	$C_L = 10 \text{ pF}$	3.2	4.5	6.2	ns
t_{PLH}	Differential propagation delay, low to high ⁽¹⁾	$V_{ID} = 200 \text{ mV}$	3.0	4.5	6.2	ns
t_{SKD1}	Differential pulse skew ⁽¹⁾			0.1		ns

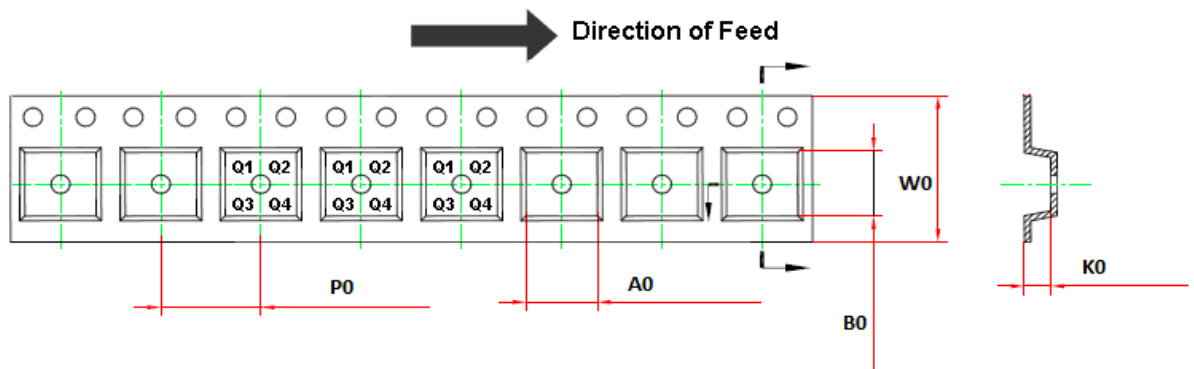
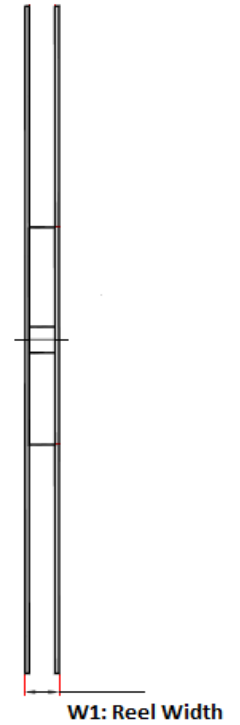
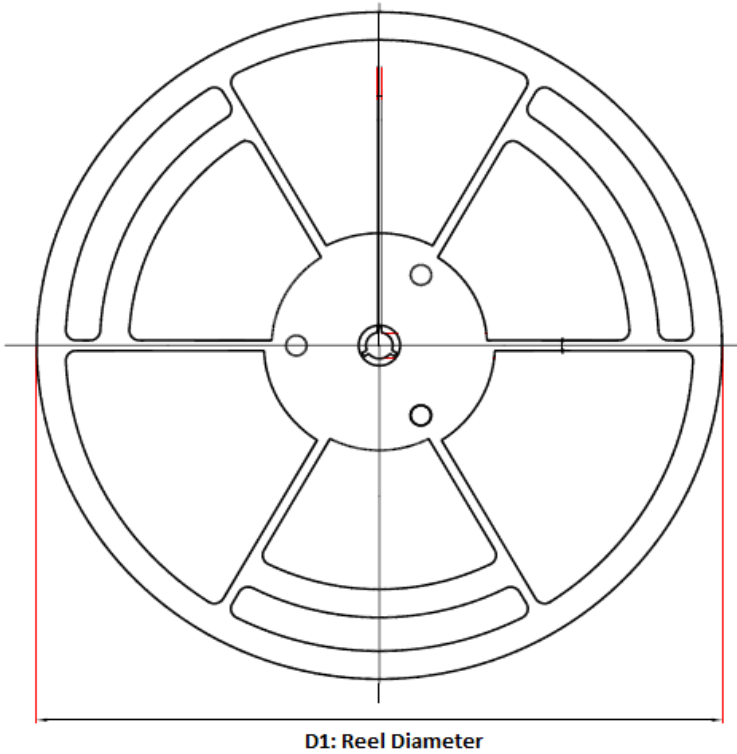
Multipoint-LVDS Line Driver and Receiver

	tPHLD – tPLHD			
tskd2	Differential channel-to-channel skew ⁽¹⁾	Same device	0.1 2.0	ns
tskd3	Differential part-to-part skew ⁽¹⁾	Different device	0.1 2.0	ns
tTLH	Rise time		1.0	ns
tTHL	Fall time		1.0	ns
tpHZ	Disable time high to Z	R _L = 2 kΩ	6	ns
tplZ	Disable time low to Z	C _L = 10 pF	6	ns
tpZH	Enable time Z to high		6	ns
tpZL	Enable time Z to low		4	ns
fMAX	Maximum operating frequency ⁽⁷⁾	All channels switching	200	MHz

Note:

(1): Spec limit is based on bench characterization and design simulation

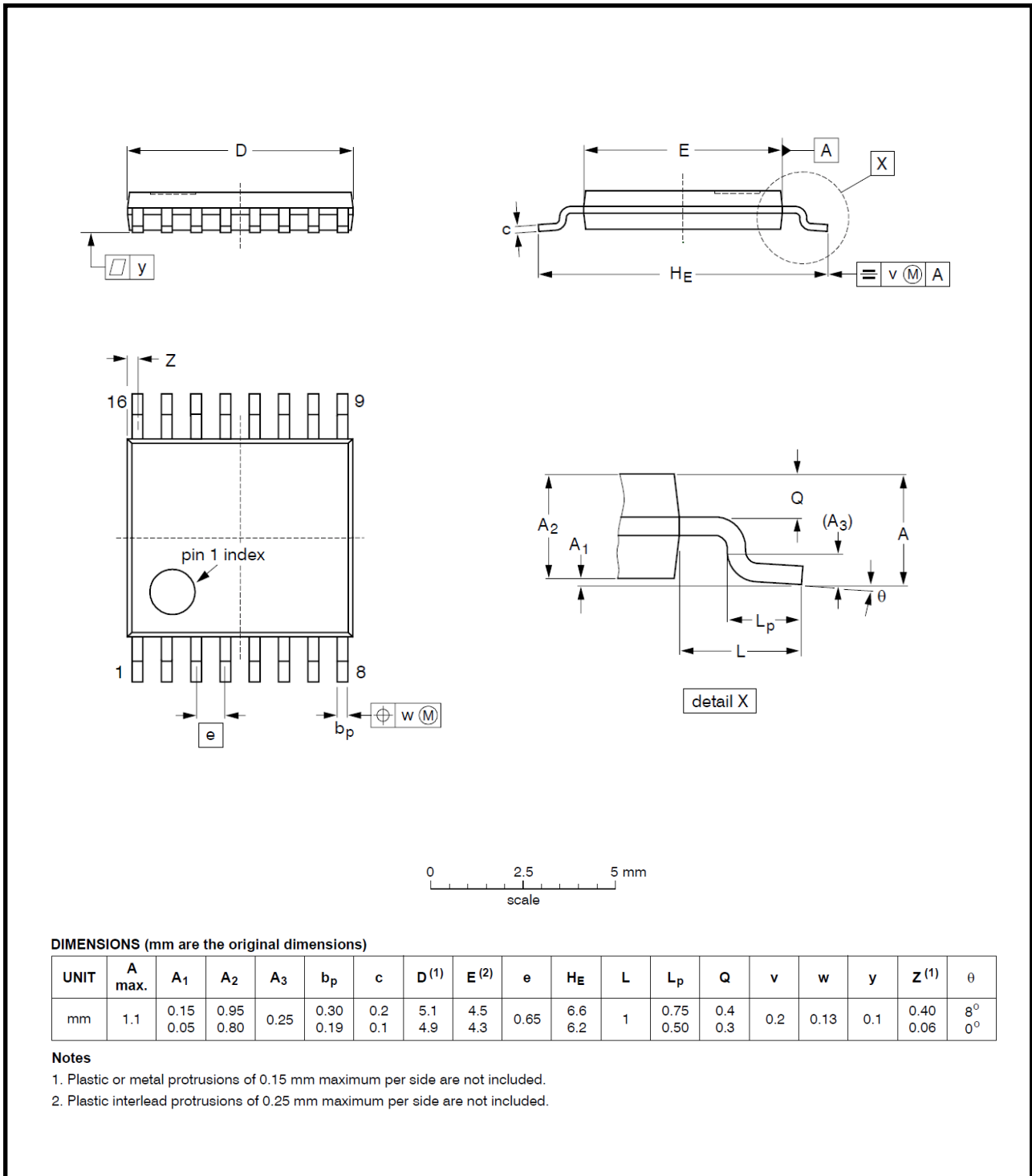
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPT9L484L1-TSR-S	TSSOP16	330	17.6	6.8±0.1	5.4±0.1	1.3±0.1	8.0±0.1	12.0±0.1	Q1

Package Outline Dimensions

TSR (TSSOP16)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

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