Nano Power Supervisory Circuits with Programmable Reset Delay

Features

- Wide-Supply Voltage Range: 1.6 V to 6.0 V
- Ultra-Low Quiescent Current: 400 nA typ
- Fixed Threshold Voltage from 1.6 V to 5 V
- Adjustable Version with Low Threshold Voltage 0.405 V (min)
- Power-on Reset Generator with Adjustable Delay Time from 30 μs to 6.2 s
- High Threshold Accuracy 1% Typ
- Manual Reset ($\overline{MR}$) Input
- Four Output Topologies：
  - TPV8348LD: active-low ($\overline{RESET}$), open-drain
  - TPV8348HD: active-high (RESET), open-drain
  - TPV8348LP: active-low ($\overline{RESET}$), push-pull
  - TPV8348HP: active-high (RESET), push-pull
- Temperature Range: −40°C to 125°C
- Green Product, SOT23-5 and DFN1.5X1-6 Packages

Applications

- Server and Data Center
- Surveillance and IP Camera
- Network Switches and Routers
- Solid State Drive
- Optical Communication Module

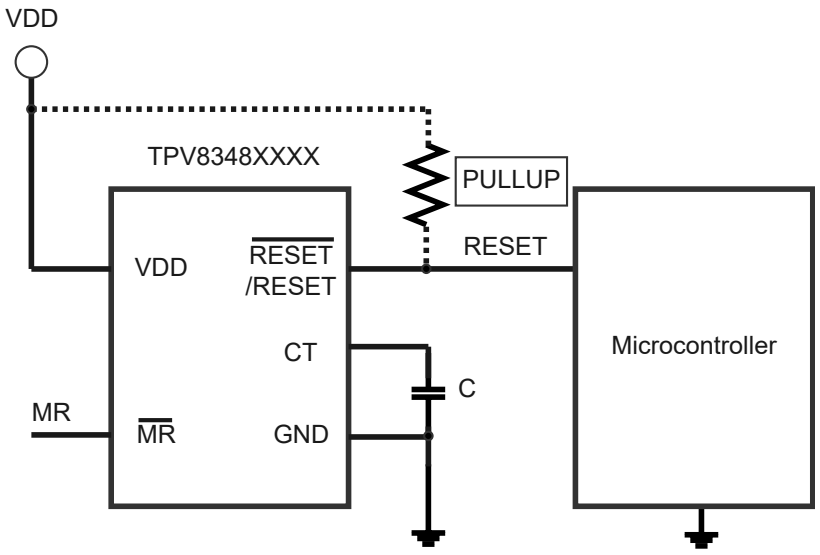
Description

The TPV8348 is a family of supervisory circuits to monitor a voltage rail, asserting an active low or active high $\overline{RESET}$ /RESET output when the voltage of the VDD pin (Fixed version) or SENSE pin (Adjustable version) drops below the threshold or when the manual reset pin $\overline{MR}$ is logic low. The $\overline{RESET}$ /RESET output remains low or high for the duration of the delay time after the detected voltage returns above the threshold with a hysteresis or manual reset $\overline{MR}$ returns to logic high. The delay time can be set by an external capacitor.

The threshold voltage of the TPV8348 device can achieve 1% accuracy. The delay time can be set to 30 μs to 6.2 s by connecting the external capacitor to the CT pin. The TPV8348 family has a very low typical quiescent current of 400 nA.

The TPV8348 is available in SOT23-5 and DFN1.5x1-6 packages. Its operating temperature range is from −40°C to +125°C.

Typical Application Circuit



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Product Family Table

Order Number	Threshold Voltage (V_{IT})	Nominal Monitored Voltage	Marking	Package
TPV8348LD160-S5TR (1)	1.6 V	1.8 V	Y16	SOT23-5
TPV8348LD220-S5TR (1)	2.2 V	2.5 V	Y22	SOT23-5
TPV8348LD270-S5TR (1)	2.7 V	3.0 V	Y27	SOT23-5
TPV8348LD290-S5TR (1)	2.9 V	3.2 V	Y29	SOT23-5
TPV8348LP290-S5TR (1)	2.9 V	3.2 V	W29	SOT23-5
TPV8348LD300-S5TR (1)	3.0 V	3.3 V	Y30	SOT23-5
TPV8348LD400-S5TR (1)	4.0 V	4.3 V	Y40	SOT23-5
TPV8348LD420-S5TR (1)	4.2 V	4.5 V	Y42	SOT23-5
TPV8348LD450-S5TR (1)	4.5 V	4.8 V	Y45	SOT23-5
TPV8348LD460-S5TR (1)	4.6 V	4.9 V	Y46	SOT23-5
TPV8348LDADJ-S5TR (1)	0.405 V	Adjustable	LDJ	SOT23-5
TPV8348HDADJ-S5TR (1)	0.405 V	Adjustable	HDJ	SOT23-5
TPV8348LPADJ-S5TR (1)	0.405 V	Adjustable	LPJ	SOT23-5
TPV8348HPADJ-S5TR (1)	0.405 V	Adjustable	HPJ	SOT23-5
TPV8348LDADJ-DFNR (1)	0.405 V	Adjustable	LDJ	DFN1.5X1.0-6
TPV8348HDADJ-DFNR (1)	0.405 V	Adjustable	HDJ	DFN1.5X1.0-6
TPV8348LPADJ-DFNR (1)	0.405 V	Adjustable	LPJ	DFN1.5X1.0-6
TPV8348HPADJ-DFNR	0.405V	Adjustable	HPJ	DFN1.5X1.0-6

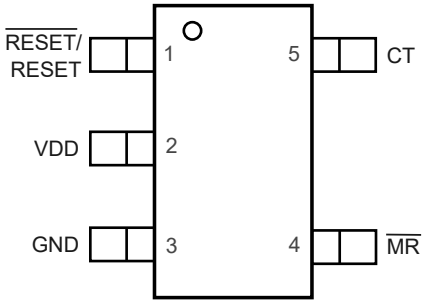
(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

Date	Revision	Notes
2020-08-05	Rev.Pre.0	Pre-Release Version.
2021-04-25	Rev.Pre.1	Added Package DFN1.5X1.0-6.
2021-05-08	Rev.Pre.2	Modified Pin Map of DFN1.5X1.0-6.
2021-10-18	Rev.Pre.3	Changed POD of SOT23-5.
2022-07-25	Rev.Pre.4	Updated as per latest datasheet format, and updated VIT accuracy in EC table.
2022-08-16	Rev.Pre.5	Updated ESD CDM.
2022-12-20	Rev.A.0	Updated feature list.

Pin Configuration and Functions

TPV8348
SOT23-5 Package
Top View



TPV8348
DFN1.5X1-6 Package
Top View

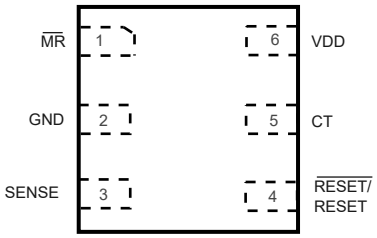


Table 1. Pin Functions: TPV8348

Pin		Name	I/O	Description
SOT23-5	DFN1.5X 1-6			
2	6	VDD	P	Supply Voltage. A 0.1-μF ceramic capacitor placed as close as to VDD pin.
-	3	SENSE	I	Sense Pin. It is used for monitoring voltage. If the voltage drops below the threshold voltage V_{IT}, the $\overline{RESET}$/RESET is asserted. The SENSE pin can be connected to any voltage by configuring an external resistor divider.
5	5	CT	I/O	Reset Delay Time Programming Pin. Connecting this pin to VDD through a 40-kΩ to 200-kΩ resistor or leaving it open resulting in fixed reset delay time. Connecting this pin to ground referenced capacitor (≥ 100 pF) gives a user-programmable reset delay time.
4	1	$\overline{MR}$	I	Manual Reset Input $\overline{MR}$ low asserts $\overline{RESET}$/RESET pin. $\overline{MR}$ is internal tied to VDD by a 90-kΩ pull-up resistor.
1	4	$\overline{RESET}$/ RESET	O	$\overline{RESET}$/RESET Output. This pin is active low or active high output with open-drain or push-pull output. It is driven to low or high when the voltage of SENSE pin is lower than the threshold V_{IT}, or the $\overline{MR}$ pin is low. $\overline{RESET}$/ RESET will keep low or high for the duration of the reset delay time programmed by the CT pin after the SENSE pin is above V_{IT}or the $\overline{MR}$ pin is high.
3	2	GND	G	Ground. This pin should be connected to ground reference.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power Supply, V_{DD} to GND		−0.3	6.5	V
V_{CT}	Input Voltage for CT, $\overline{MR}$, $\overline{RESET}$/RESET pin	−0.3 to V_{DD} + 0.3 V, max 6 V		
V_{RESET}				
V_{MR}				
V_{SENSE}	Input Voltage for SENSE Pin	−0.3	6.5	V
I_{RESET}	Current of $\overline{RESET}$/RESET Pin		5	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	187	110	°C/W
DFN1.5X1-6	120	20.3	°C/W

Electrical Characteristics

All test conditions: VDD= 1.6 V to 6.0 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter			Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		−40°C < T_J < 125°C	1.6		6.0	V
$V_{DD(min)}$	Minimum VDD to Guaranteed $\overline{\text{RESET}}$/ RESET Output Valid				0.5	0.8	V
I_{DD}	Quiescent Current (I_Q)		V_{DD} = 5.5V, $\overline{\text{RESET}}$/RESET not asserted, $\overline{\text{MR}}$, $\overline{\text{RESET}}$ /RESET, CT pin open		0.4	1.5	μA
V_{OL}	Output Low Voltage of $\overline{\text{RESET}}$/RESET Pin		1.6 V ≤ V_{DD} < 6.0 V, I_{OL} = 2.0 mA			0.3	V
V_{OH}	Output low voltage of $\overline{\text{RESET}}$/RESET pin		1.6 V ≤ V_{DD} < 6.0 V, I_{OL} = 2.0 mA	0.8 VDD			V
$V_{IT,ERR}$	Negative-going Input Threshold Accuracy		−40°C < T_J < 125°C	−3	1	3	%
V_{HYS}	Hysteresis on V_{IT}				1.5		%
R_{MR}	MR Internal Pull-up Resistance				90		kΩ
I_{SENSE}	Input Current at SENSE Pin		V_{SENSE} = V_{IT}		10		nA
			V_{SENSE} = 5.5 V		110		nA
C_{IN}	Input Capacitance, any pin	CT pin	V_{IN} = 0 V to V_{DD}		5		pF
		Other pins	V_{IN} = 0 V to 6.0 V		5		pF
V_{IL}	$\overline{\text{MR}}$ Logic Low Input			0		0.3V_{DD}	V
V_{IH}	$\overline{\text{MR}}$ Logic High Input			0.7V_{DD}			V
t_w	Input Pulse Width to Assert $\overline{\text{RESET}}$/RESET Pin	SENSE	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		12		μs
		$\overline{\text{MR}}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		300		ns
t_D	Reset Delay Time	C_T = Open	Guaranteed by design and characterization		30		μs
		C_T = 10 nF			6.2		ms
		C_T = 1 μF			619		ms
t_{MR}	Propagation Delay from $\overline{\text{MR}}$to RESET	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$/ RESET	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		300		ns
t_{RP}	Propagation Delay from SENSE to RESET	SENSE to $\overline{\text{RESET}}$/ RESET	V_{IH} = 1.05 V_{DD}, V_{IL} = 0.95 V_{DD}		12		μs

Detailed Description

Overview

The TPV8348 is a family of supervisory circuits to monitor a voltage rail, asserting an active low or active high $\overline{\text{RESET}}$ / RESET output when the voltage of the VDD pin (Fixed version) or sense pin (Adjustable version) drops below a fixed threshold or when the manual reset pin $\overline{\text{MR}}$ is logic low. The $\overline{\text{RESET}}$ /RESET output remains low or high for the duration of the delay time after the detected voltage returns above the threshold with a hysteresis or manual reset $\overline{\text{MR}}$ returns to logic high. The delay time can be set by an external capacitor.

Functional Block Diagram

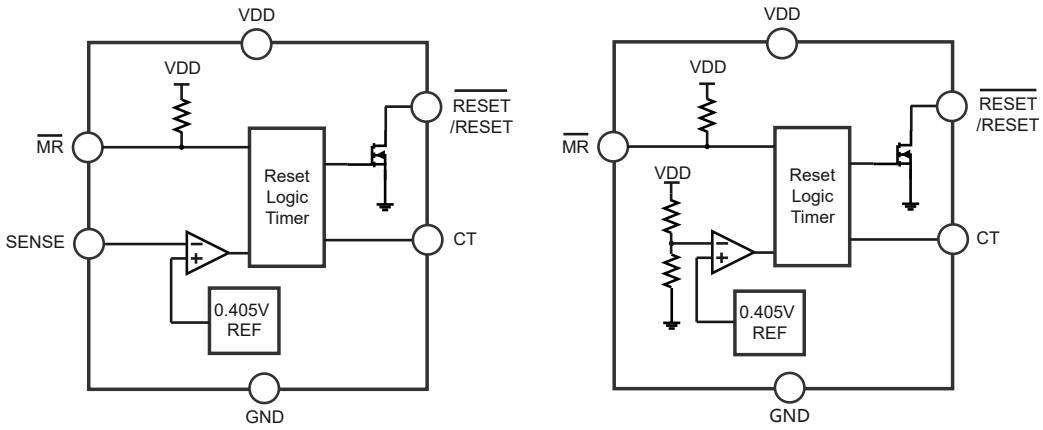


Figure 1. Functional Block for TPV8348 Adjustable Version and Fixed Version

Feature Description

RESET Output

The reset threshold voltage can be set by the factory from 1.6 V to 5 V or be set to any voltage above 0.405 V using an external resistor divider. The sense pin monitors the system voltage. If the voltage on this pin drops below V_{IT}, the $\overline{RESET}$ /RESET is asserted.

The TPV8348 features an active-low or active-high output. For active-low output, the reset signal is guaranteed to be logic low for VSENSE down to V_{IT}. For active-high output, the reset signal is guaranteed to be logic high for VSENSE down to V_{IT}. Reset remains asserted for the duration of the reset delay time (t_D) after VSENSE rises above the reset threshold. Figure 2 shows the reset outputs.

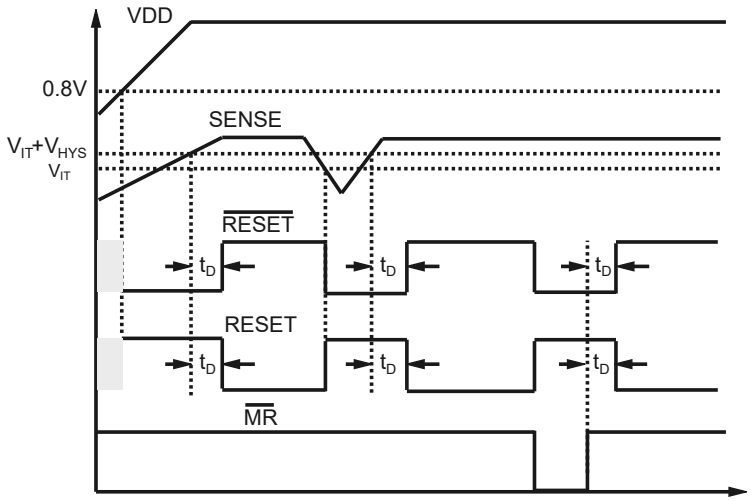


Figure 2. SENSE Reset and MR Reset Timing

RESET Delay Time

The TPV8348 provides programmable reset delay time (t_D), which is realized by selecting a capacitor between CT and GND to allow the designer to set any reset delay time from 30 μs to 6.2 s. The reset delay time (t_D) under given capacitor value is calculated using Equation 1.

$$t_D\,(\mu s) = 600 \times C_{CT}\,(nF) \quad (1)$$

Manual RESET ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a microcontroller to initiate a reset. A logic low on $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to logic high and SENSE is above the reset threshold, $\overline{RESET}$ is de-asserted after the reset delay time. $\overline{MR}$ can be left unconnected if not used.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Figure 3 shows the typical application circuit of TPV8348 with a reset threshold voltage set by the external resistor divider. Figure 4 shows the application circuit of TPV8348 with a reset threshold voltage set by the factory.

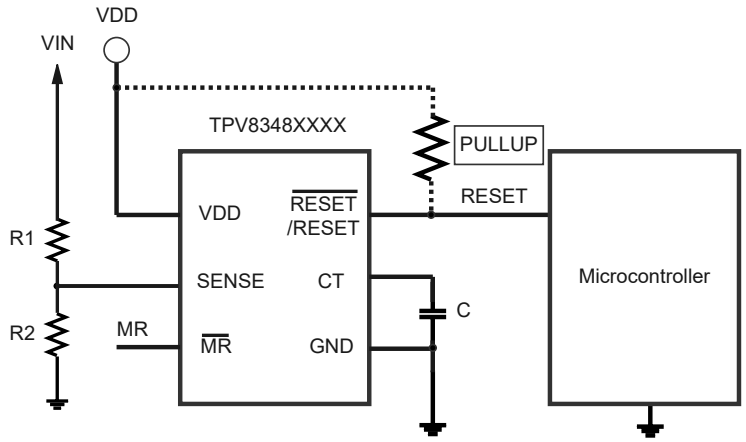


Figure 3. TPV8348 Adjustable Version Typical Application Circuit

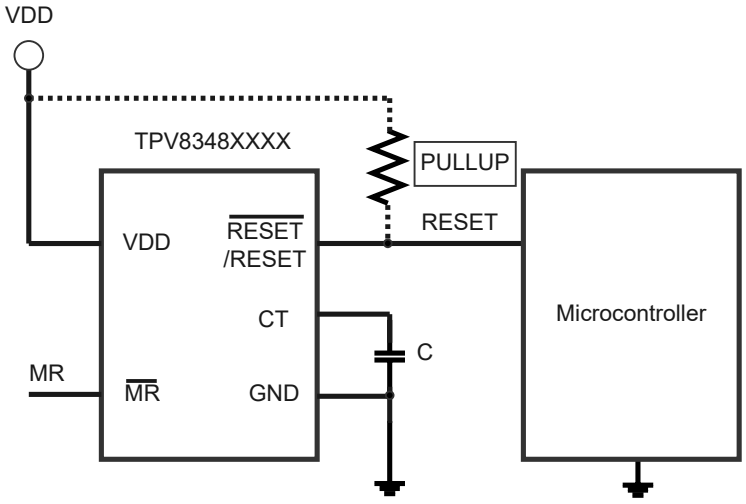
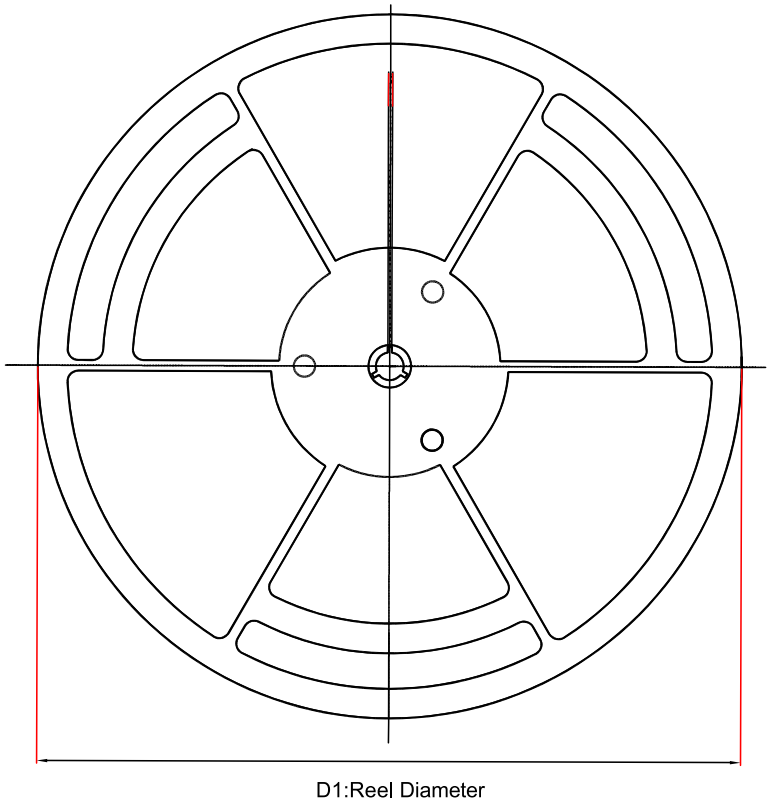
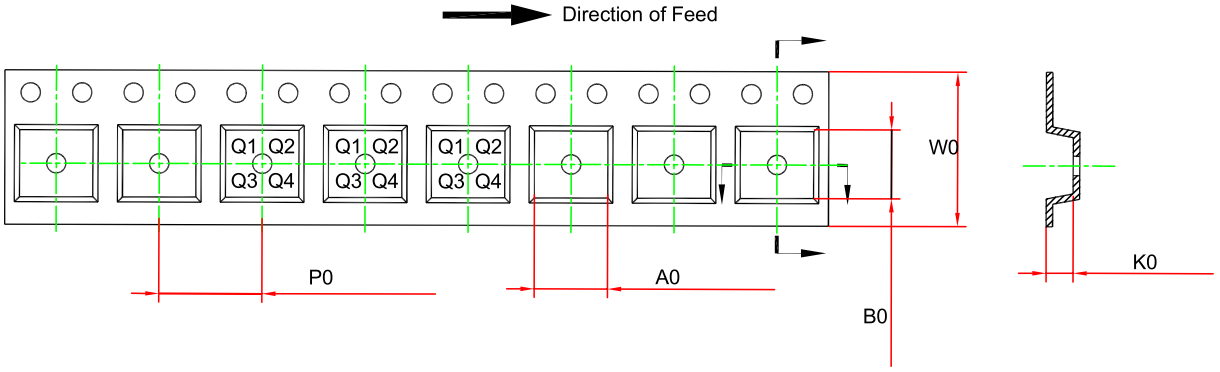


Figure 4. TPV8348 Fixed Version Typical Application Circuit

Tape and Reel Information



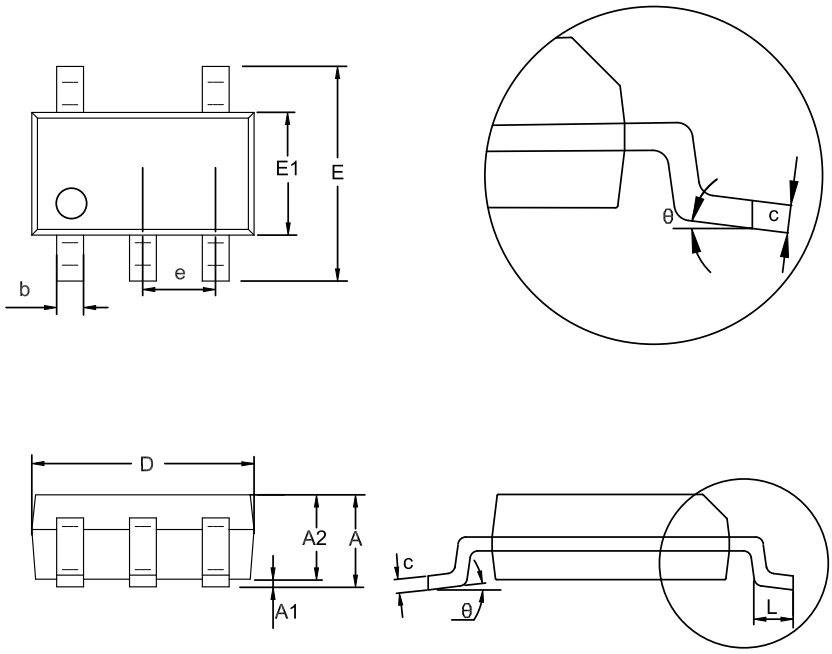


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV8348xxxx-S5TR	SOT23-5	179	9	3.3	3.2	1.4	4	8	Q3
TPV8348xxxx-DFNR	DNF1.5X1.0-6	178	10	1.15	1.72	0.7	4	8	Q1

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



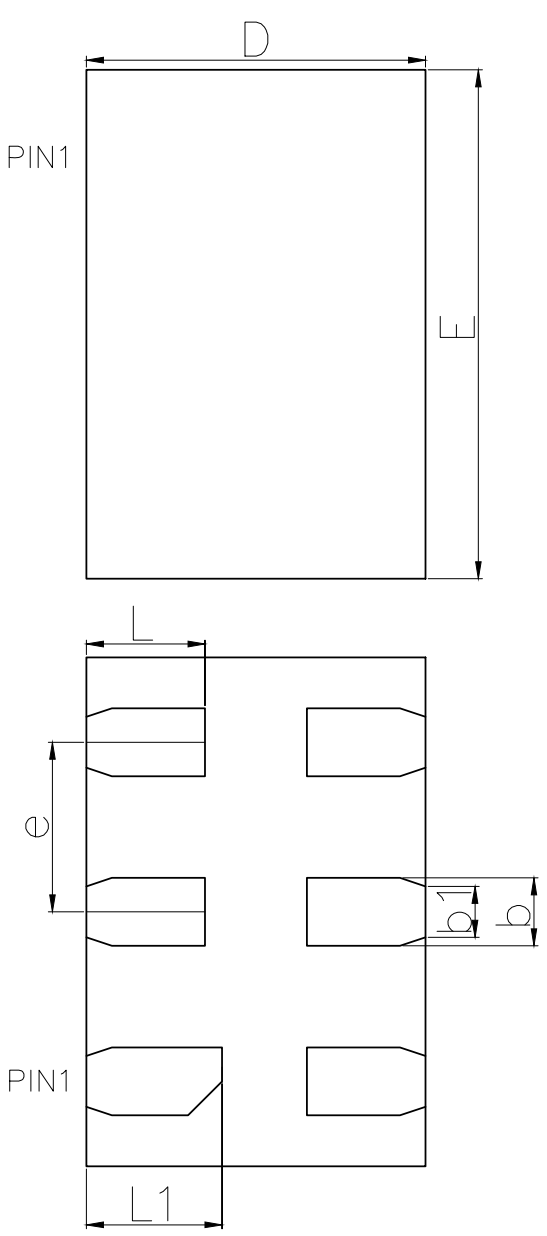
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

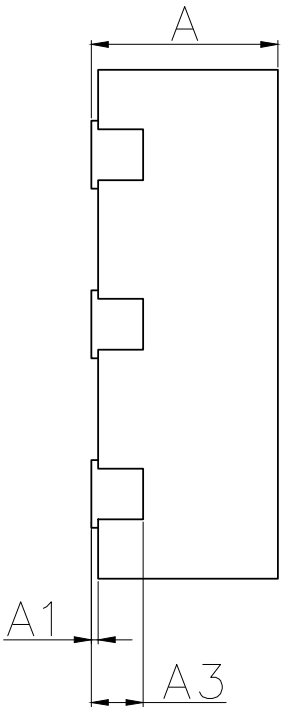
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN1.5X1-6

Package Outline Dimensions DFN(DFN1.5X1-6-A)





NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
b1	0.150 REF		0.006 REF	
A3	0.100	0.200	0.004	0.008
D	0.900	1.100	0.035	0.043
E	1.400	1.600	0.055	0.063
e	0.500 BSC		0.020 BSC	
L	0.274	0.426	0.011	0.017
L1	0.324	0.476	0.013	0.019

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV8348LD160-S5TR	−40 to 125°C	SOT23-5	Y16	3	Tape and Reel, 3000	Green
TPV8348LD220-S5TR	−40 to 125°C	SOT23-5	Y22	3	Tape and Reel, 3000	Green
TPV8348LD270-S5TR	−40 to 125°C	SOT23-5	Y27	3	Tape and Reel, 3000	Green
TPV8348LD290-S5TR	−40 to 125°C	SOT23-5	Y29	3	Tape and Reel, 3000	Green
TPV8348LP290-S5TR	−40 to 125°C	SOT23-5	W29	3	Tape and Reel, 3000	Green
TPV8348LD300-S5TR	−40 to 125°C	SOT23-5	Y30	3	Tape and Reel, 3000	Green
TPV8348LD400-S5TR	−40 to 125°C	SOT23-5	Y40	3	Tape and Reel, 3000	Green
TPV8348LD420-S5TR	−40 to 125°C	SOT23-5	Y42	3	Tape and Reel, 3000	Green
TPV8348LD450-S5TR	−40 to 125°C	SOT23-5	Y45	3	Tape and Reel, 3000	Green
TPV8348LD460-S5TR	−40 to 125°C	SOT23-5	Y46	3	Tape and Reel, 3000	Green
TPV8348LDADJ-S5TR	−40 to 125°C	SOT23-5	LDJ	3	Tape and Reel, 3000	Green
TPV8348HDADJ-S5TR	−40 to 125°C	SOT23-5	HDJ	3	Tape and Reel, 3000	Green
TPV8348LPADJ-S5TR	−40 to 125°C	SOT23-5	LPJ	3	Tape and Reel, 3000	Green
TPV8348HPADJ-S5TR	−40 to 125°C	SOT23-5	HPJ	3	Tape and Reel, 3000	Green
TPV8348LDADJ-DFNR	−40 to 125°C	DFN1.5X1.0-6	LDJ	3	Tape and Reel, 4000	Green
TPV8348HDADJ-DFNR	−40 to 125°C	DFN1.5X1.0-6	HDJ	3	Tape and Reel, 4000	Green
TPV8348LPADJ-DFNR	−40 to 125°C	DFN1.5X1.0-6	LPJ	3	Tape and Reel, 4000	Green
TPV8348HPADJ-DFNR	−40 to 125°C	DFN1.5X1.0-6	HPJ	3	Tape and Reel, 4000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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